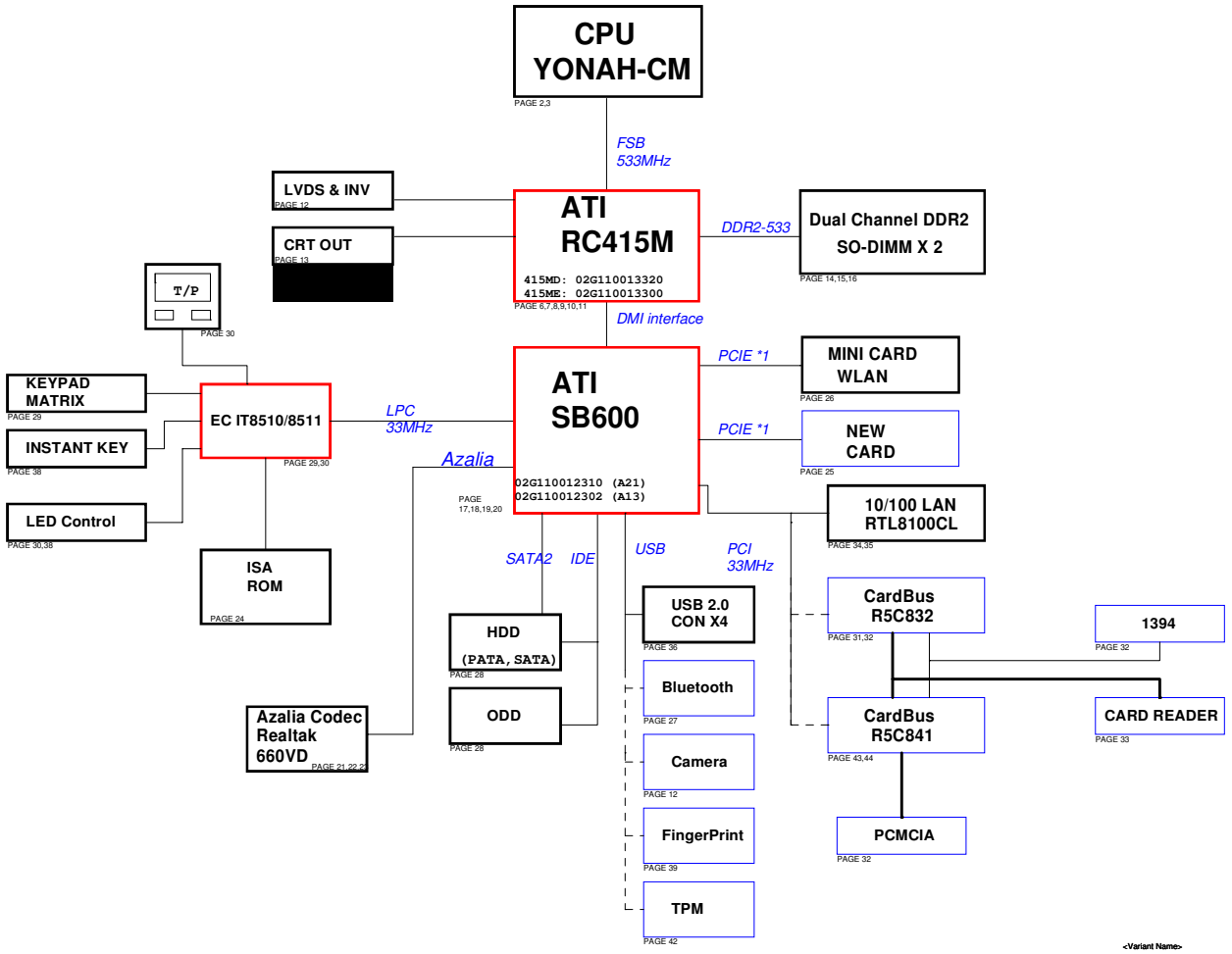
T12R Serier Block Diagram



<Variant Name>

Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 1 of 63

+VCCP_AGTL+ @ +VCCP
JP201
SHORT_PIN
2.5A
+VCCP +VCCP 5,6,10,17,19,20,52
+VCCP_AGTL+ +VCCP_AGTL+ 3

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

12G011204792==>12G04600479A
V1.1 ME

U201A
T202
R201 56Ohm
R202 54.9Ohm @
T201
T203
T204 TPC28T
R203 56Ohm @
R204 56Ohm
R205 56Ohm @
R206 56Ohm
R207 56Ohm
R208 56Ohm
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
BCLK
RESERVED
H_ADSTB#0
H_ADSTB#1
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BR0# 6
H_IERR#
H_INIT# 17
H_LOCK# 6
H_CPURST# 6
H_RS#0 6
H_RS#1 6
H_RS#2 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
+VCCP_AGTL+
GND
H_PREQ#
H_TDO
H_PROCHOT_S#
CPU_THRM_DA 4
CPU_THRM_DC 4
PM_THRMTRIP# 19
CLK_CPU_BCLK 5
CLK_CPU_BCLK# 5

U201B
H_D#[0..63] 6
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
H_DSTBN#0 6
H_DSTBP#0 6
H_DINV#0 6
H_DSTBN#1 6
H_DSTBP#1 6
H_DINV#1 6
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
GTL_REF
MISC
TEST1
TEST2
BSEL[0]
BSEL[1]
BSEL[2]
CPU_BSEL0 5
CPU_BSEL1 5
CPU_BSEL2 5
R209 1KOhm 1%
C201 0.1UF/10V @
R213 2KOhm 1%
<500 mil (55 Ohm)
T/B trace 5
Space 25
@R214 1KOhm
R216 51Ohm
R210 27.4Ohm 1%
R211 54.9Ohm 1%
R212 27.4Ohm 1%
R215 54.9Ohm 1%
H_DPRSTP# 17,50
H_DPSLP# 17
H_DPWR# 6
H_PWRGD 17
T205
H_CPUSLP#
PM_PSI# 50
H_SLP# 6,17

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

12G04600479A
12G04600479A

68 ? 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ? 5%

+VCCP_AGTL+
H_PROCHOT_S#
R217 56Ohm

<Variant Name>

Title : YONAH CPU (1)
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12RG | Rev: 2.0
Date: 星期二, 十月 07, 2007 | Sheet 2 of 63

+VCCP_AGTL+ +VCCP_AGTL+ 2
+VCORE +VCORE 50
+1.5VO +1.5VO 54

YUNAH FSB667

	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667

	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

U201C

12G04600479A

U201D

12G04600479A

+VCCA +1.5VO
JP301
1MM_OPEN_5MIL
@

+VCCP_AGTL+
+VCCA
120mA / 20mil
Close to Pin B26
C301 10UF/10V
C318 0.01UF/25V
checklist suggests
10uF POSCAP

AD6	H_VID0	1	0Ohm	2 RN302A VR_VID0 50
AE5	H_VID1	3	0Ohm	4 RN302B VR_VID1 50
AE5	H_VID2	5	0Ohm	6 RN302C VR_VID2 50
AF4	H_VID3	7	0Ohm	8 RN302D VR_VID3 50
AE3	H_VID4	1	0Ohm	2 RN303A VR_VID4 50
AF2	H_VID5	3	0Ohm	4 RN303B VR_VID5 50
AE2	H_VID6	5	0Ohm	6 RN303C VR_VID6 50
		7	0Ohm	8 RN303D

R301 100Ohm
R302 100Ohm

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

+VCORE
1215---PWR comp
Place the cap on North of Secondary side
CE301 330UF/2V N/A

Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

Place these upper side inside socket cavity on L1
C302 C303 C304 C305 C306 C307 22UF/6.3V

Place these lower side inside socket cavity on L1
C308 C309 C310 C311 C312 C313 22UF/6.3V @ / N/A

Place these upper side inside socket cavity on L6
C314 C315 C316 C317 22UF/6.3V

Place these lower side inside socket cavity on L6
C319 C320 C321 C322 22UF/6.3V @ / N/A

+VCCP_AGTL+
+1.05V Decoupling Capacitor
Place near CPU
C323 C324 C325 C326 C327 C328 c0402 0.1UF/10V
CE302 100UF/2.5V

+VCORE
C332 C333 c0402 0.1UF/10V

<Variant Name>

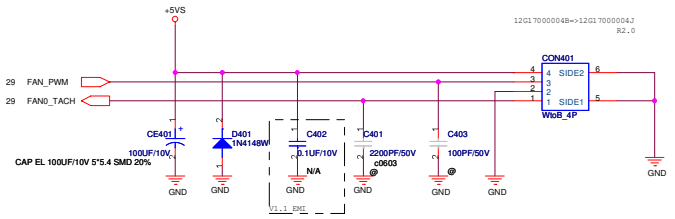
Title : Yonah CPU (2)
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12RG | Rev: 2.0
Date: 星期三, 一月 07, 2007 | Sheet 3 of 63

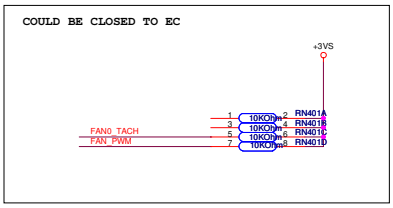
+5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS 5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

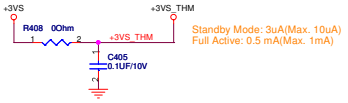
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



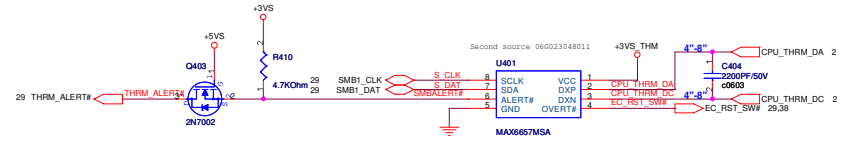




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



<Variant Name>

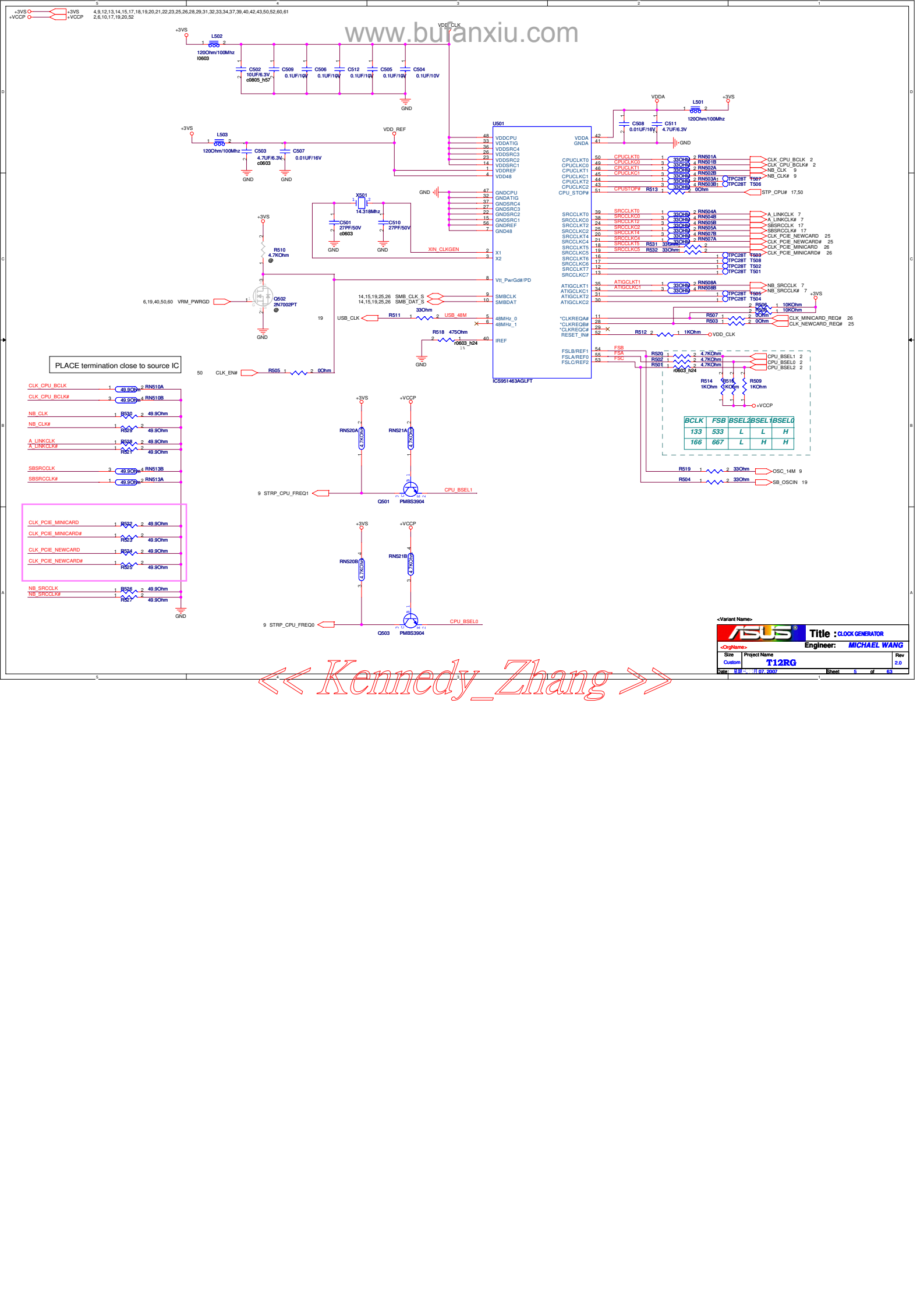
ASUSTeK COMPUTER INC

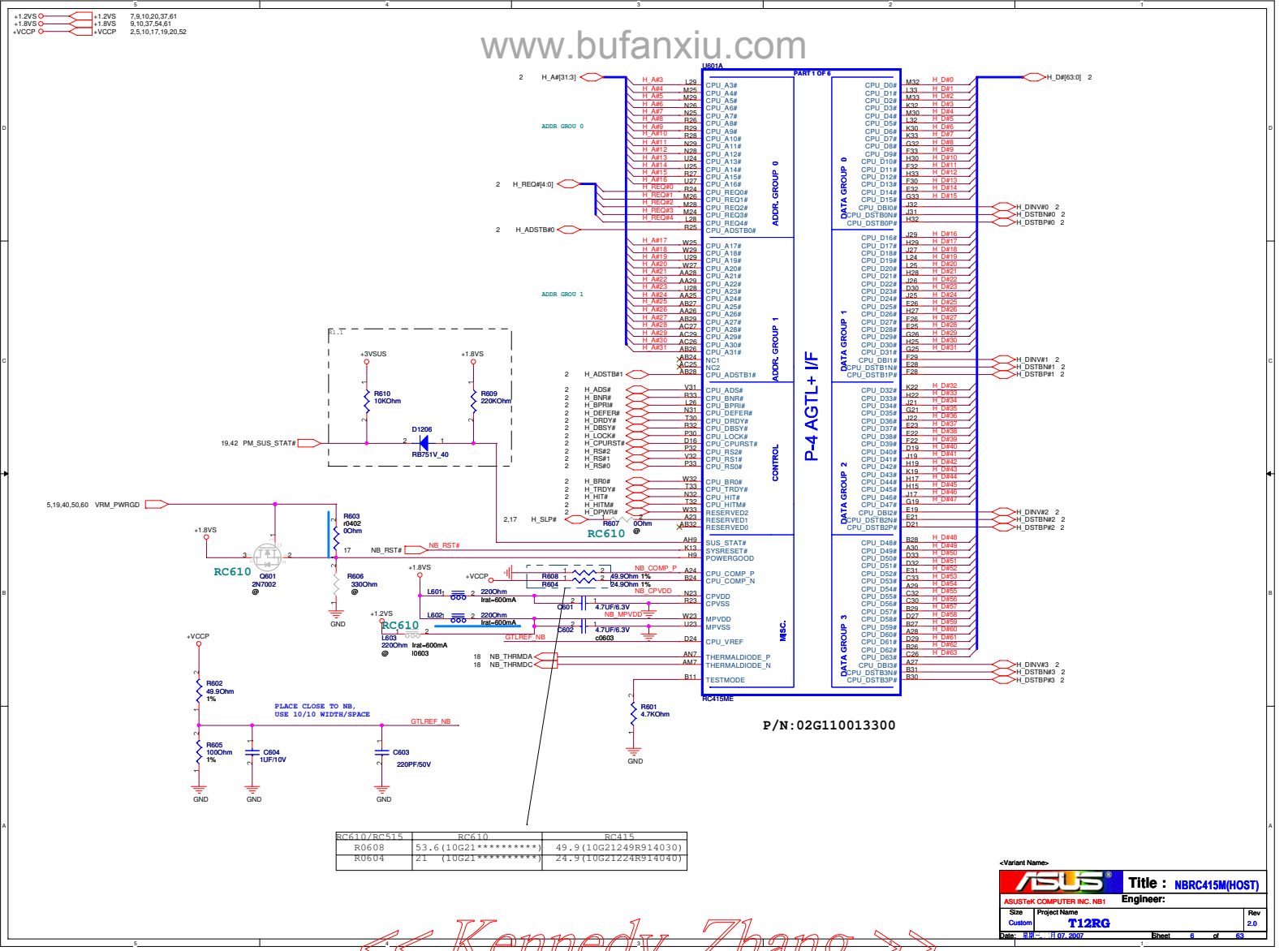
Title : THER-SENSOR,FAN

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期三, 一月 07, 2007 Sheet 4 of 63


www.buranxiu.com
U501
ICS951463AGLFT
PLACE termination close to source IC
Q502 2N7002PT
Q501 PMBS3904
Q503 PMBS3904
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GENERATOR
Engineer: MICHAEL WANG
Project Name T12RG
Rev 2.0
Sheet 5 of 63
<< Kennedy_Zhang >>



RC610/RC515	RC610	RC415
R0608	53.6(10G21**********)	49.9(10G21249R914030)
R0604	21 (10G21**********)	24.9(10G21224R914040)

<Variant Name>

ASUSTeK COMPUTER INC. NB1

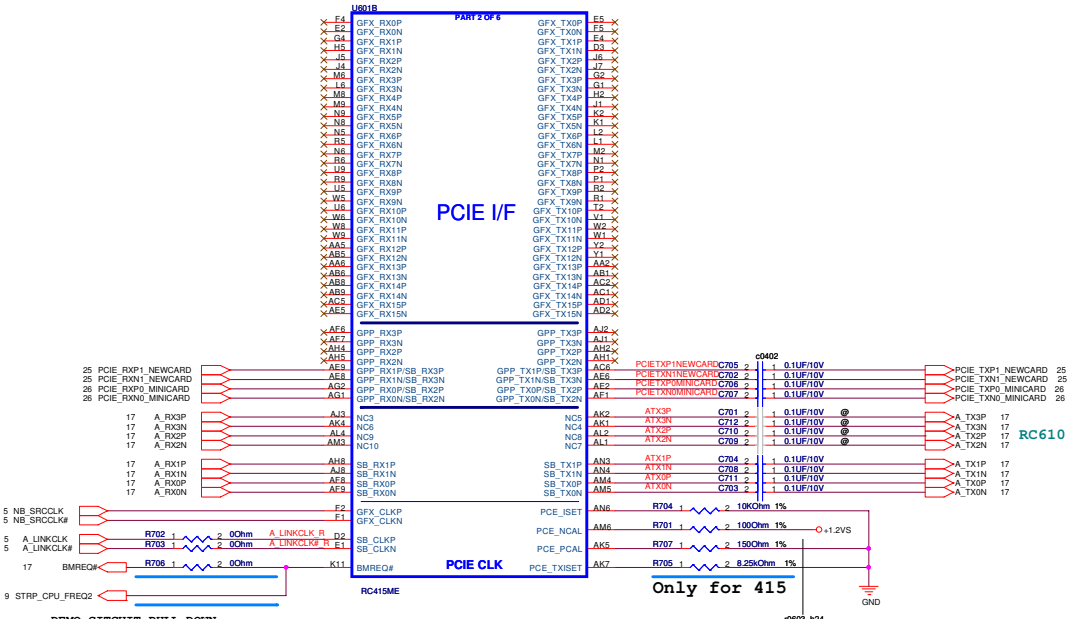
Title : NBRC415M(HOST)

Engineer:

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 6 of 63

+1.2VS +1.2VS 6,9,10,20,37,61



r0603 h24

RC610/RC515	RC610	RC415
R0704	1.47K(10G21*********)	10K(10G2131002130 30)
R0701	2K (10G21*********)	100(10G2131000130 10)
R0707	562 (10G21*********)	150(10G2131500130 30)

<Variant Name>

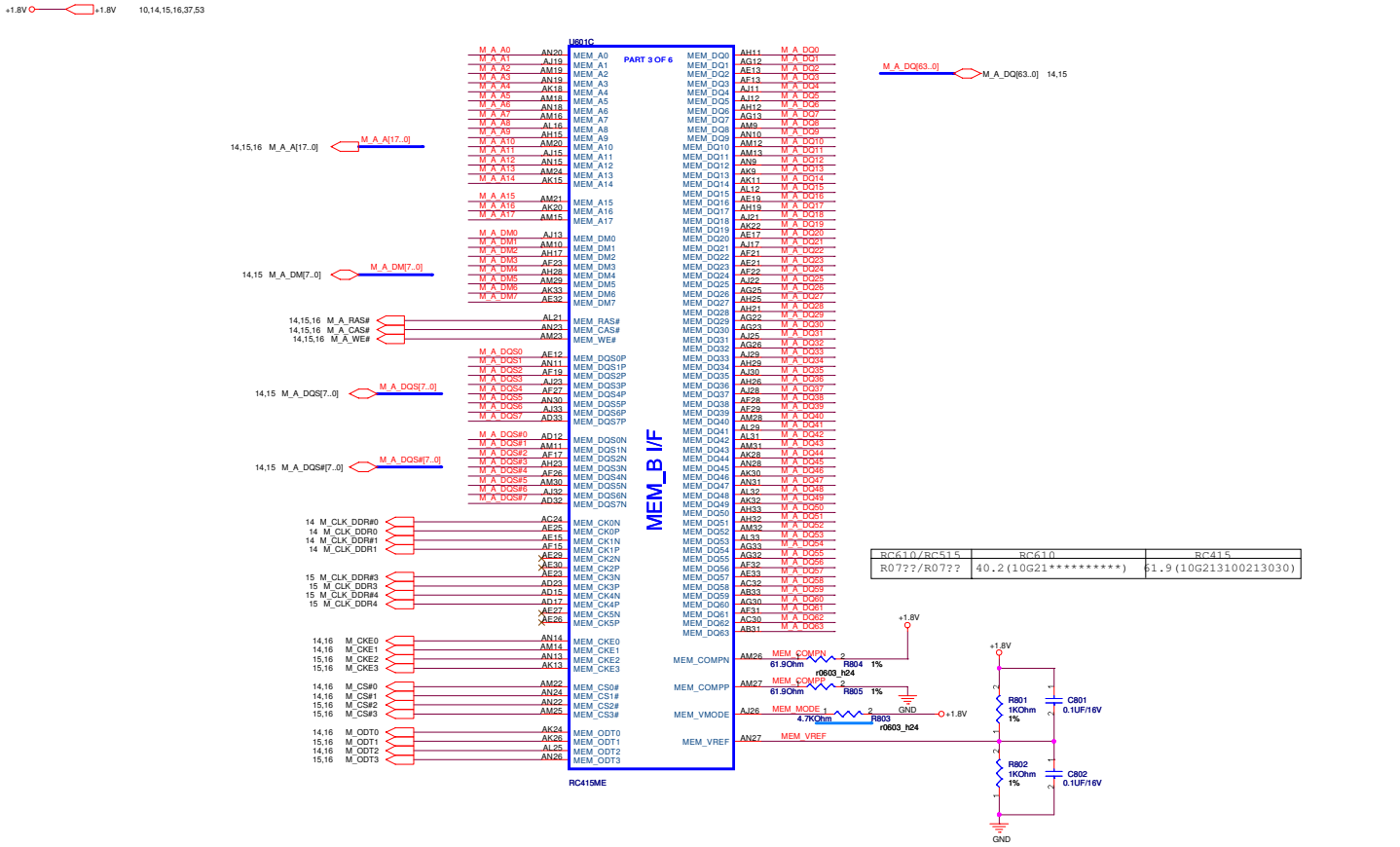
ASUSTeK COMPUTER INC. NB1

Title : NB-945PM(DMI & CFG)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

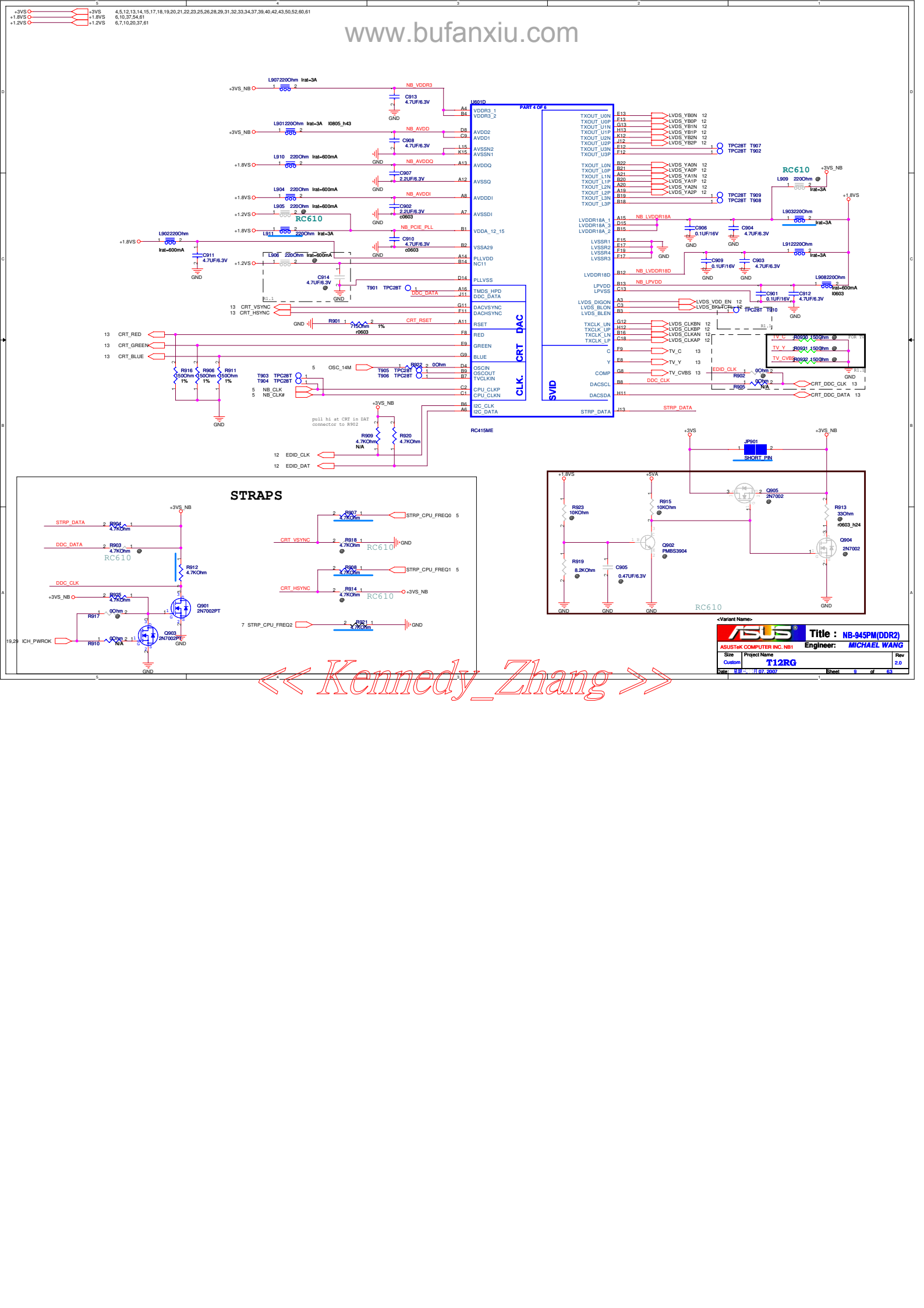
Date: 星期二, 一月 07, 2007 Sheet 7 of 63

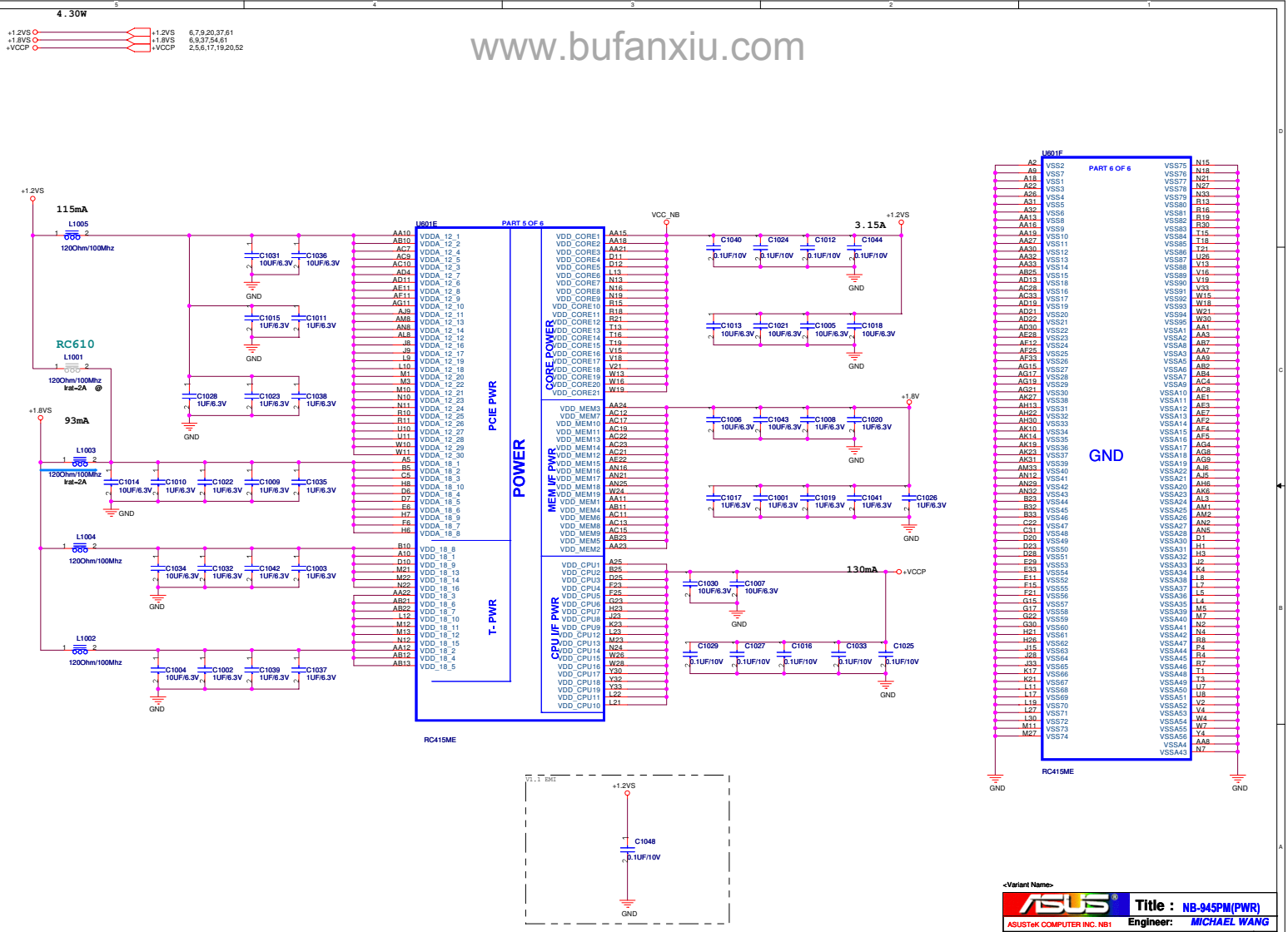


RC610/RC515	RC610	RC415
R07??/R07??	40.2(10G21*********)	61.9(10G2131002130 30)

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_945PM(PCI-E)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 8 of 63	





<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(PWR)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 10 of 63	

<Variant Name>

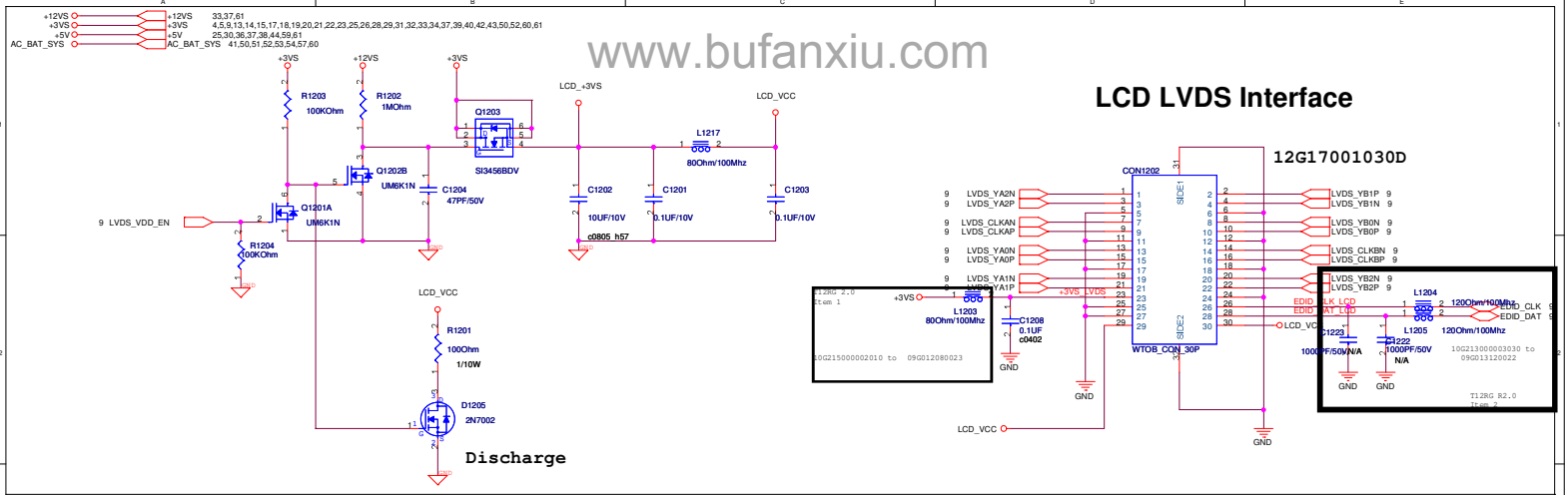
Title : HISTORY

ASUSTeK COMPUTER INC

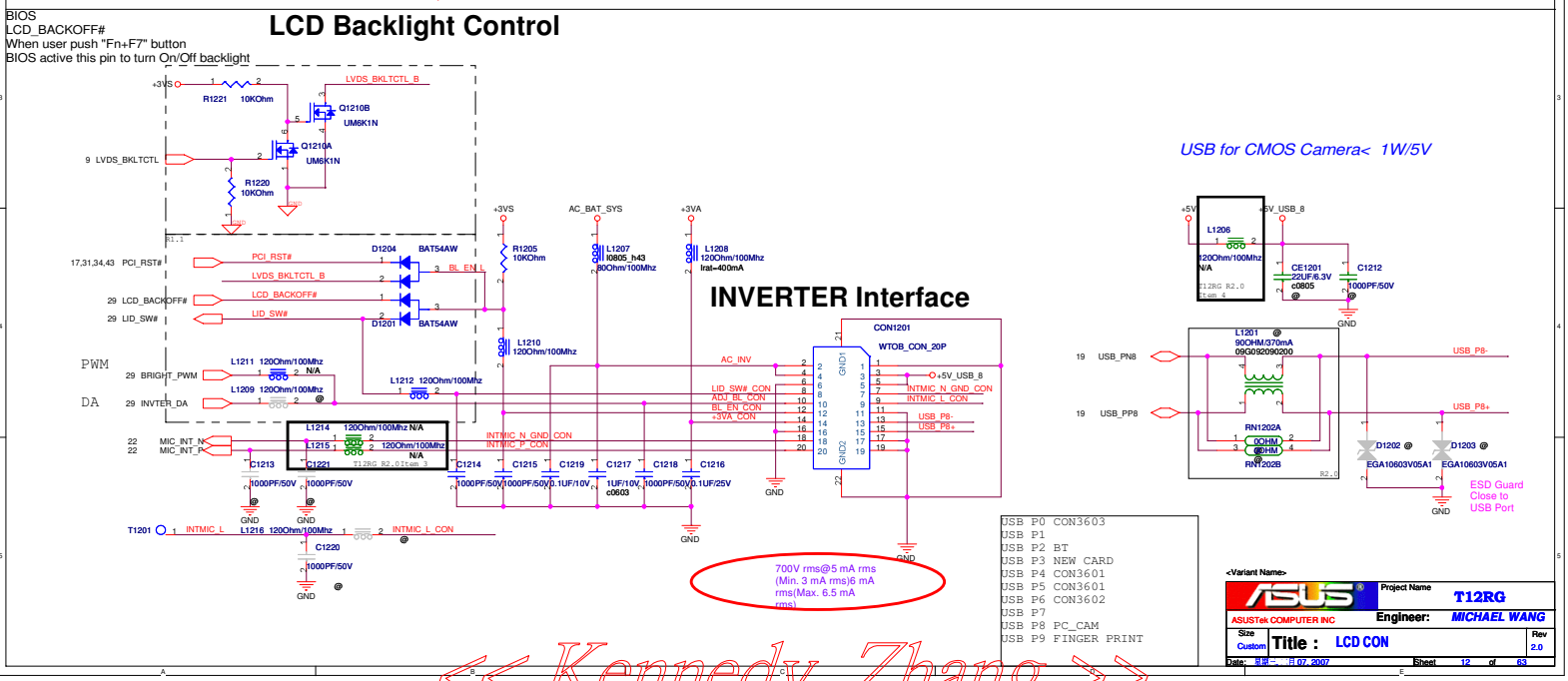
Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 11 of 63



BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight



USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT

ESD Guard Close to USB Port

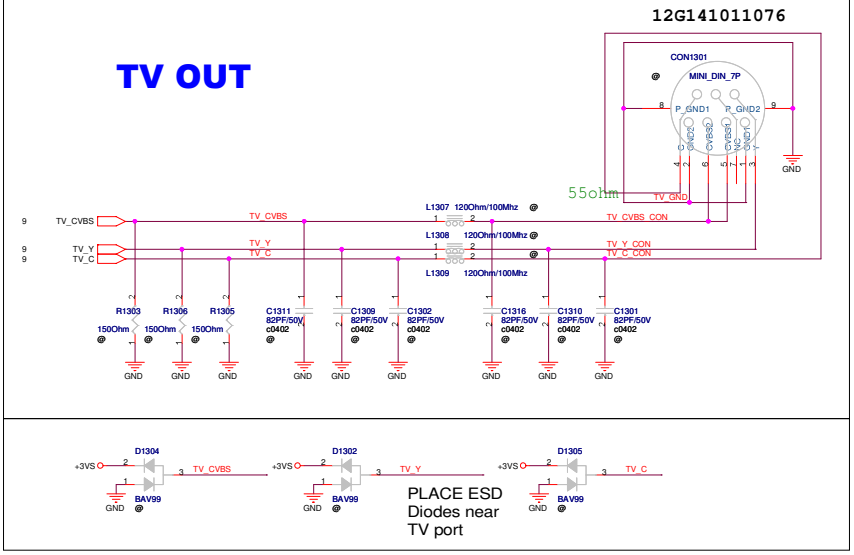
<Variant Name>

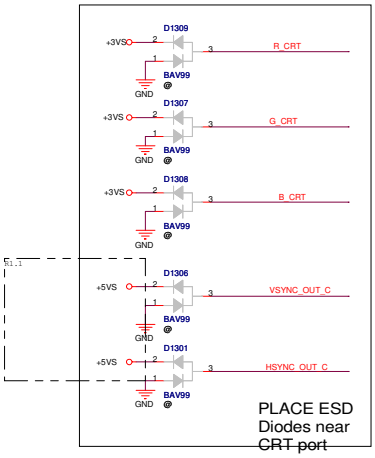
ASUSTek COMPUTER INC	Project Name	T12RG	
	Engineer:	MICHAEL WANG	
Size: Custom	Title :	LCD CON	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet	12 of 63	

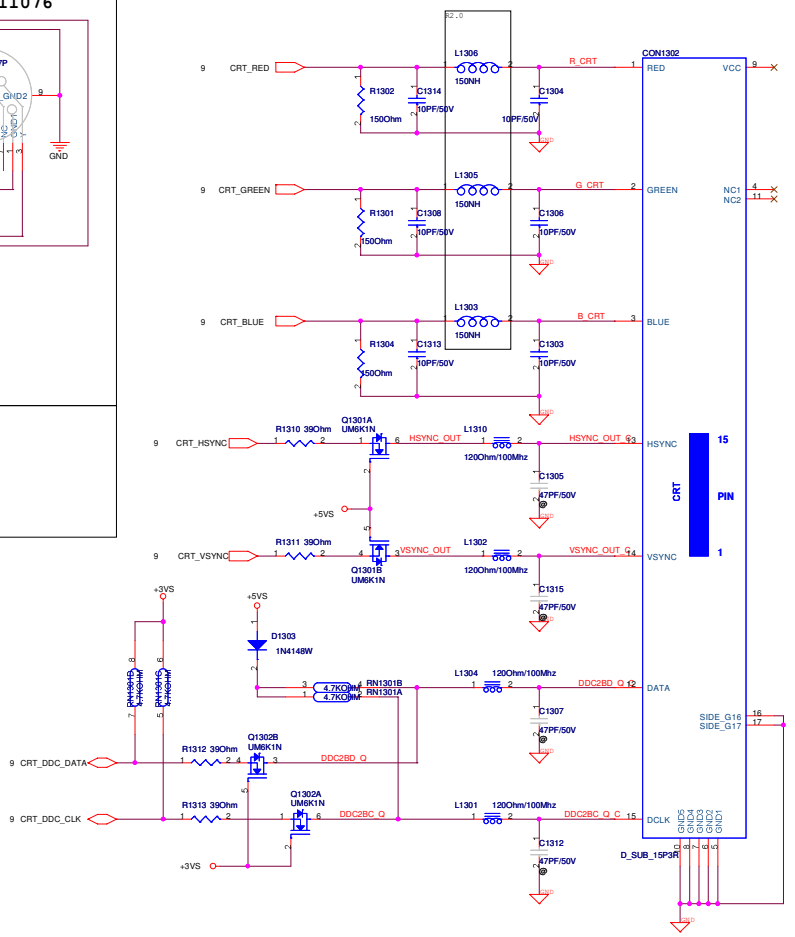
12G101102152
=>12G10110215A

12G141011076

TV OUT







<Variant Name>

ASUSTeK COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 13 of 63	

+3VS
+1.8V
+3VS
+1.8V
4,5,9,12,13,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,15,16,37,53

FRON

PN:12G02502200E==>12G025022004
V1.1 ME second source

M_CLK_DDR0
C1401
68 Ohm/0402
N/A
M_CLK_DDR#0

M_CLK_DDR1
C1402
68 Ohm/0402
N/A
M_CLK_DDR#1

CON1401A

8,15,16 M_A_A[17:0]
M_A_A0 102
M_A_A1 101
M_A_A2 100
M_A_A3 99
M_A_A4 98
M_A_A5 97
M_A_A6 94
M_A_A7 92
M_A_A8 93
M_A_A9 91
M_A_A10 105
M_A_A11 90
M_A_A12 89
M_A_A13 116
M_A_A14 86
M_A_A17 84
85
M_A_A15 107
M_A_A16 106

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2
BA0 BA1
S0# S1#
CK0 CK0# CK1 CK1#
CKE0 CKE1
CAS# RAS# WE#
SA0 SA1
SCL SDA
ODT0 ODT1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_A_DQ0 5
M_A_DQ1 7
M_A_DQ2 17
M_A_DQ3 19
M_A_DQ4 4
M_A_DQ5 6
M_A_DQ6 16
M_A_DQ7 18
M_A_DQ8 23
M_A_DQ9 25
M_A_DQ10 35
M_A_DQ11 37
M_A_DQ12 20
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M_A_DQ20 44
M_A_DQ21 46
M_A_DQ22 56
M_A_DQ23 58
M_A_DQ24 61
M_A_DQ25 63
M_A_DQ26 73
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M_A_DQ28 62
M_A_DQ29 64
M_A_DQ30 74
M_A_DQ31 76
M_A_DQ32 123
M_A_DQ33 125
M_A_DQ34 135
M_A_DQ35 137
M_A_DQ36 124
M_A_DQ37 126
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M_A_DQ41 143
M_A_DQ42 151
M_A_DQ43 153
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M_A_DQ48 157
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M_A_DQ50 173
M_A_DQ51 175
M_A_DQ52 158
M_A_DQ53 160
M_A_DQ54 174
M_A_DQ55 176
M_A_DQ56 179
M_A_DQ57 181
M_A_DQ58 189
M_A_DQ59 191
M_A_DQ60 180
M_A_DQ61 182
M_A_DQ62 192
M_A_DQ63 194

M_A_DQ[63..0] 8,15

8,16 M_CS#0
8,16 M_CS#1
8 M_CLK_DDR1
8 M_CLK_DDR0
8 M_CLK_DDR#1
8,16 M_CKE0
8,16 M_CKE1
8,15,16 M_A_CAS#
8,15,16 M_A_RAS#
8,15,16 M_A_WE#
110
115
30
32
164
166
79
80
113
108
109
198
200
197
195
5,15,19,25,26 SMB_CLK_S
5,15,19,25,26 SMB_DAT_S
8,16 M_ODT0
8,16 M_ODT2
8,15 M_A_DM[7:0]
114
119
M_A_DM0 10
M_A_DM1 28
M_A_DM2 52
M_A_DM3 67
M_A_DM4 130
M_A_DM5 147
M_A_DM6 170
M_A_DM7 185
8,15 M_A_DQS[7:0]
M_A_DQS0 13
M_A_DQS1 31
M_A_DQS2 51
M_A_DQS3 70
M_A_DQS4 131
M_A_DQS5 148
M_A_DQS6 169
M_A_DQS7 188
8,15 M_A_DQS#[7:0]
M_A_DQS#0 11
M_A_DQS#1 29
M_A_DQS#2 49
M_A_DQS#3 68
M_A_DQS#4 129
M_A_DQS#5 146
M_A_DQS#6 167
M_A_DQS#7 186

DDR2_DIMM_200P

+1.8V
C1403 2.2UF/6.3V
C1404 2.2UF/6.3V
C1405 2.2UF/6.3V
C1406 2.2UF/6.3V
C1407 2.2UF/6.3V
C1408 0.1UF/10V
C1409 0.1UF/10V
C1410 0.1UF/10V
C1411 0.1UF/10V
+3VS
C1412 2.2UF/6.3V
C1413 0.1UF/10V
15,16 M_VREF_DIMM0
C1414 2.2UF/6.3V
C1415 0.1UF/10V

CON1401B

112 VDD1
111 VDD2
117 VDD3
96 VDD4
95 VDD5
118 VDD6
81 VDD7
82 VDD8
87 VDD9
103 VDD10
88 VDD11
104 VDD12
199 VDDSPD
83 NC1
120 NC2
50 NC3
69 NC4
163 NCTEST
1 VREF
201 GND0
202 GND1
203 NP_NC1
204 NP_NC2
47 133 183 77 12 48 184 78 71 72 121 122 196 193 8 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
18 24 41 53 42 54 59 65 60 66 127 139 128 145 165 171 172 177 187 178 190 9 21 33 155 34 132 144 156 168 2 3 15 27 39 149 161 28 40 138 150 162 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

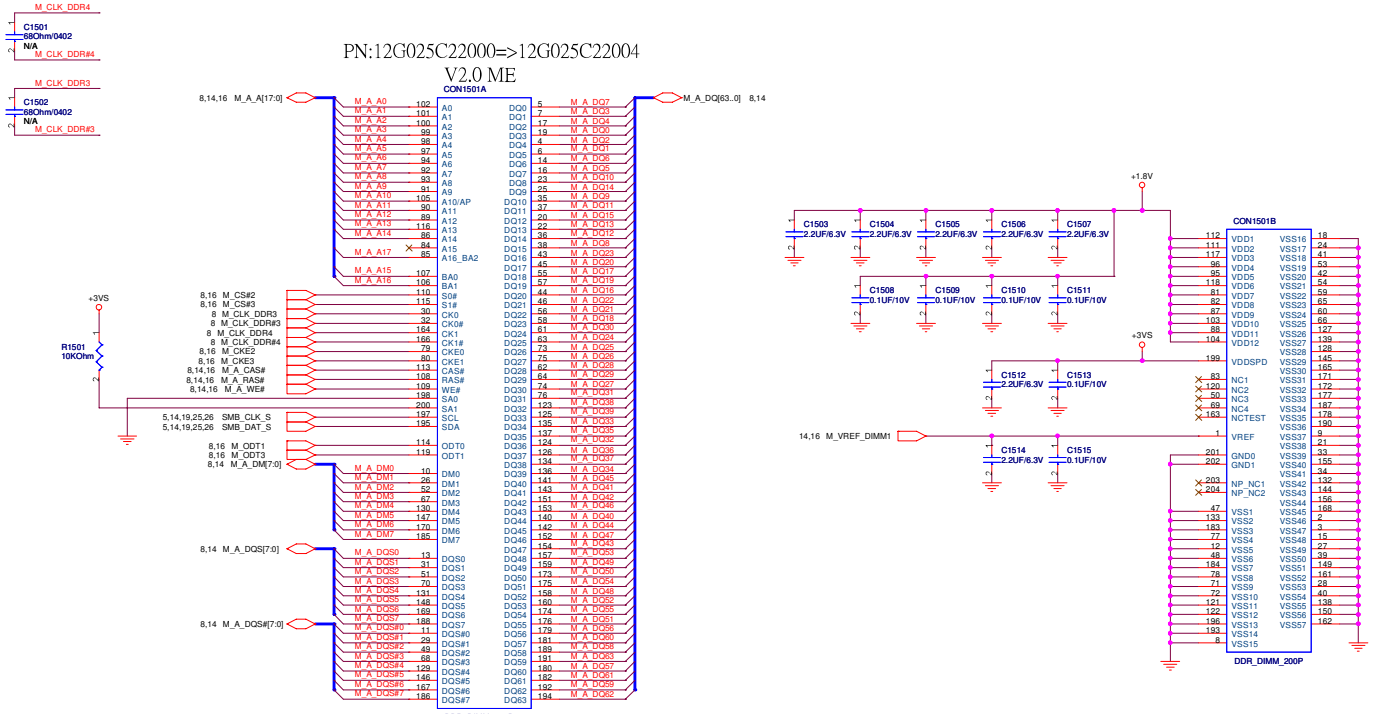
DDR2_DIMM_200P

<Variant Name>

Title : DDR2 SO-DIMM1
ASUSTeK COMPUTER INC. NB1
Engineer: MICHAEL WANG
Size: Custom
Project Name: T12RG
Rev: 2.0
Date: 星期一, 一月 07, 2007
Sheet 14 of 63

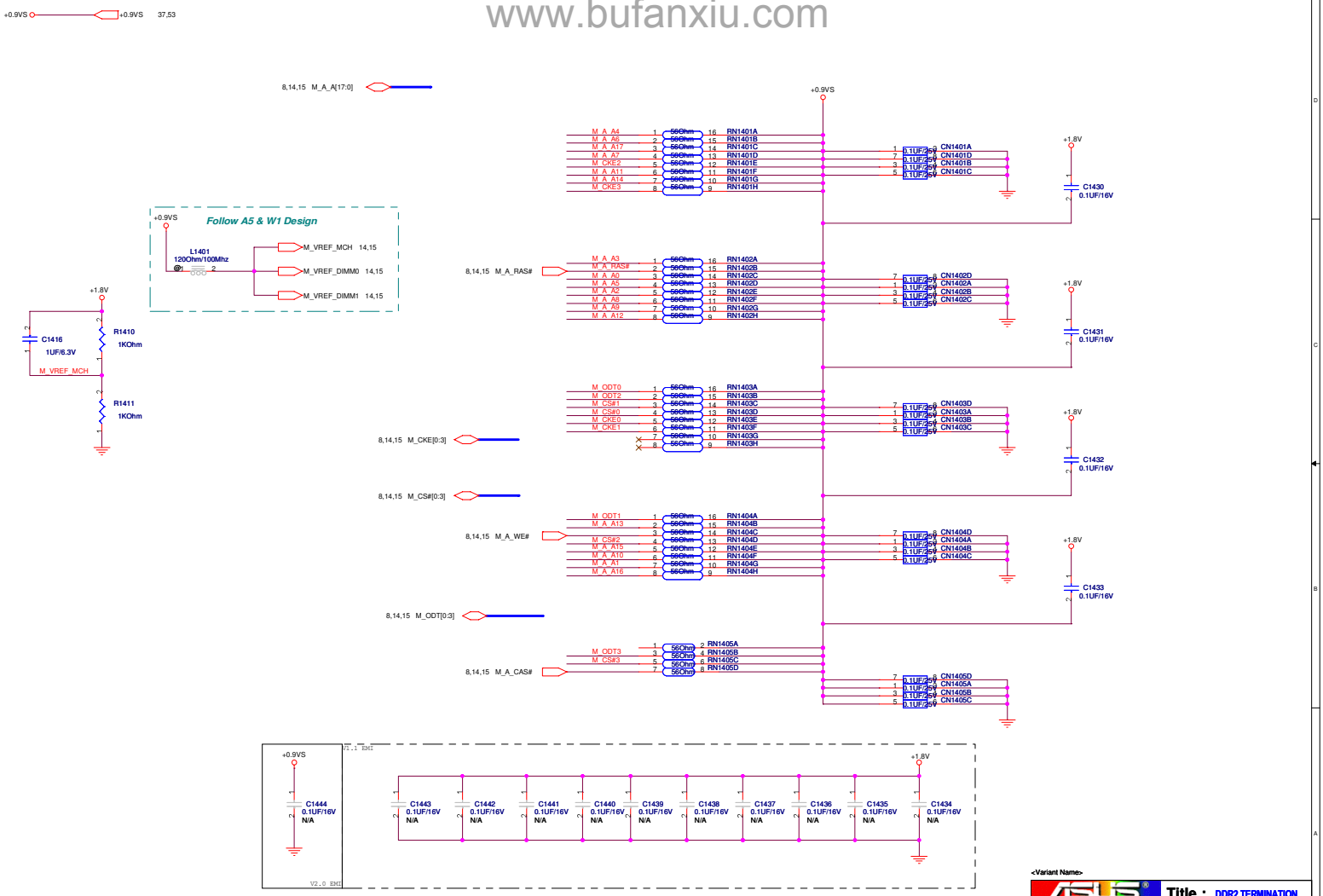
+3VS
+1.8V
+3VS
+1.8V
4,5,9,12,13,14,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,14,16,37,53

PN:12G025C22000=>12G025C22004
V2.0 ME



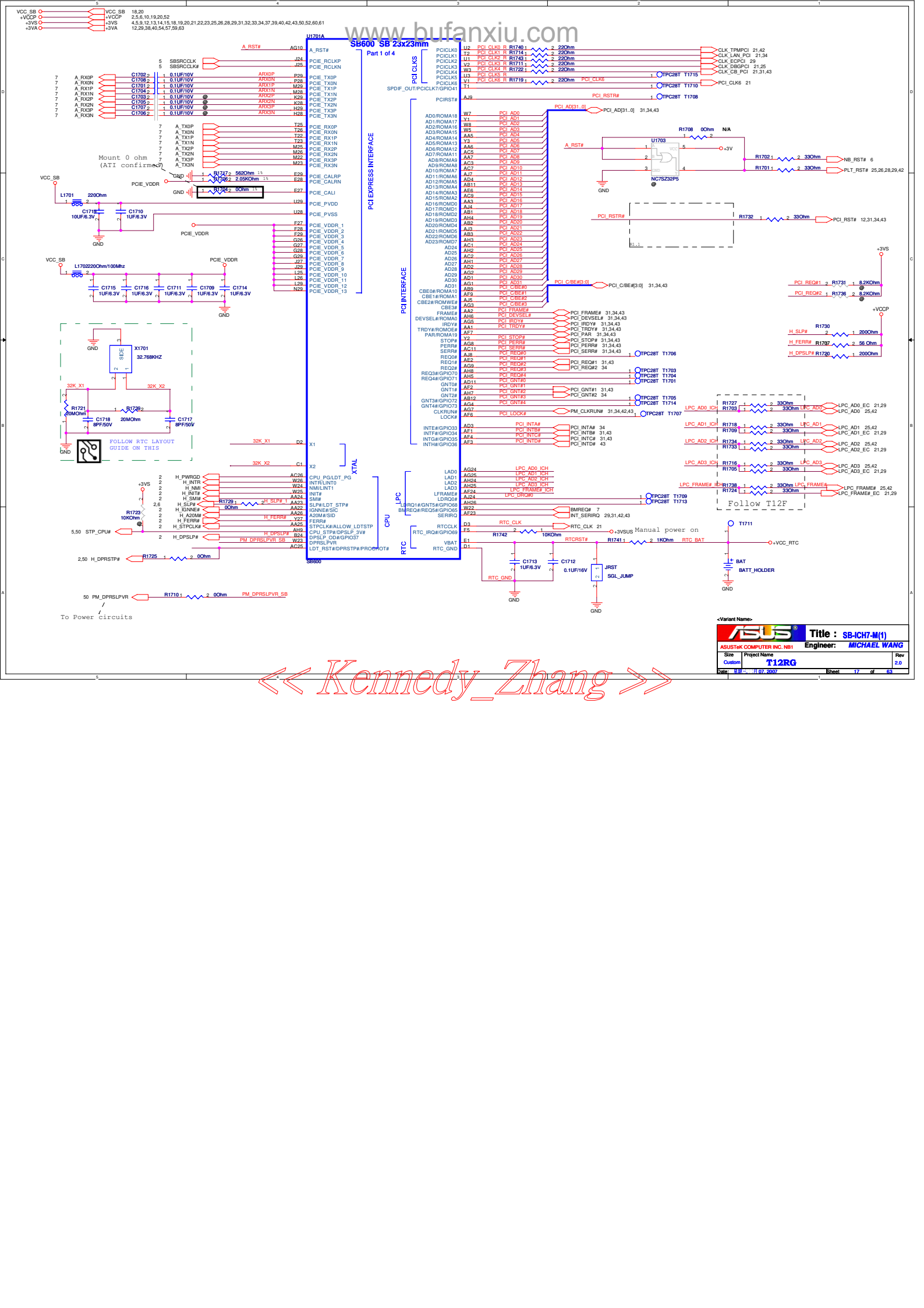
<Variant Name>

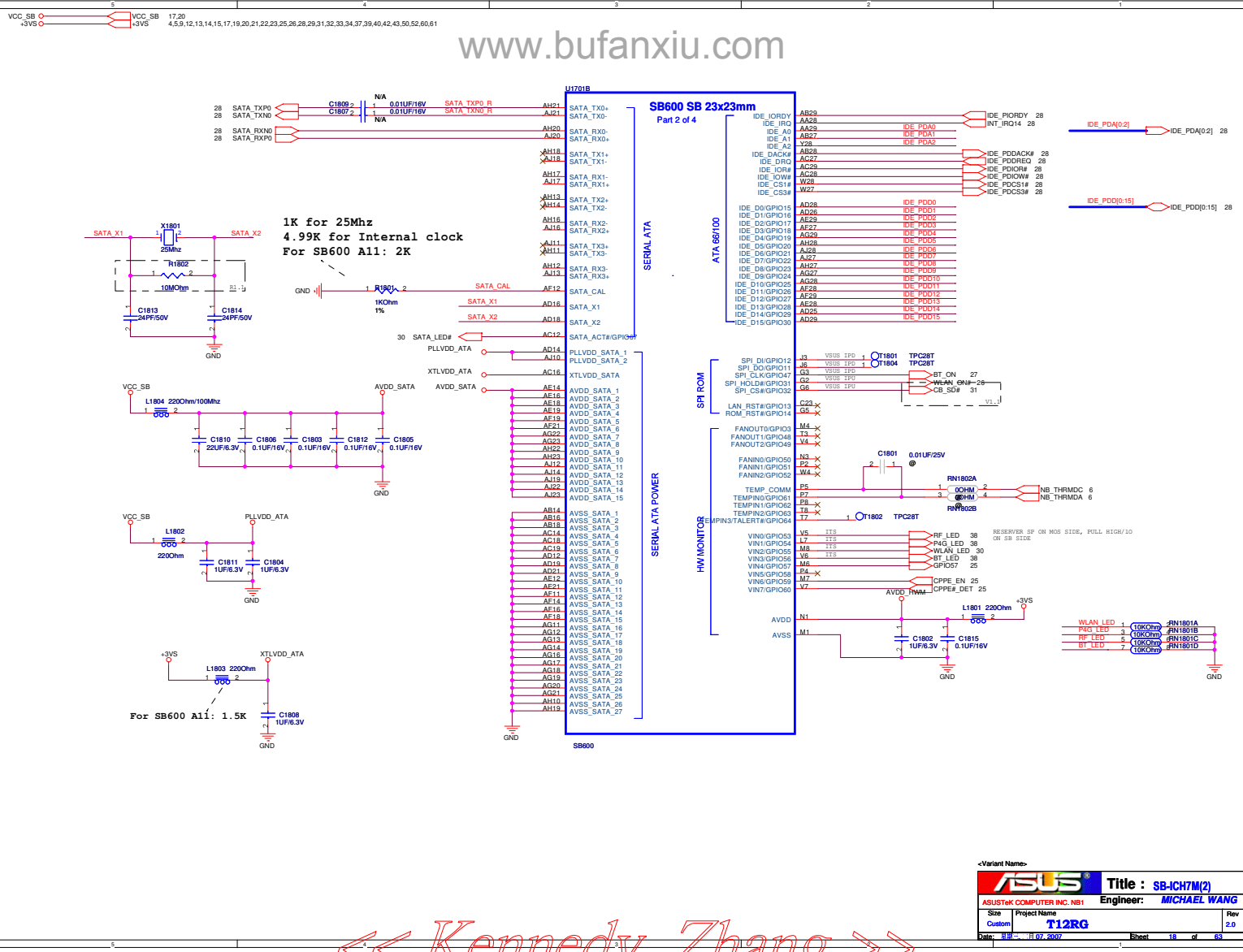
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 三月 07, 2007	Sheet 15 of 63	



<Variant Name>

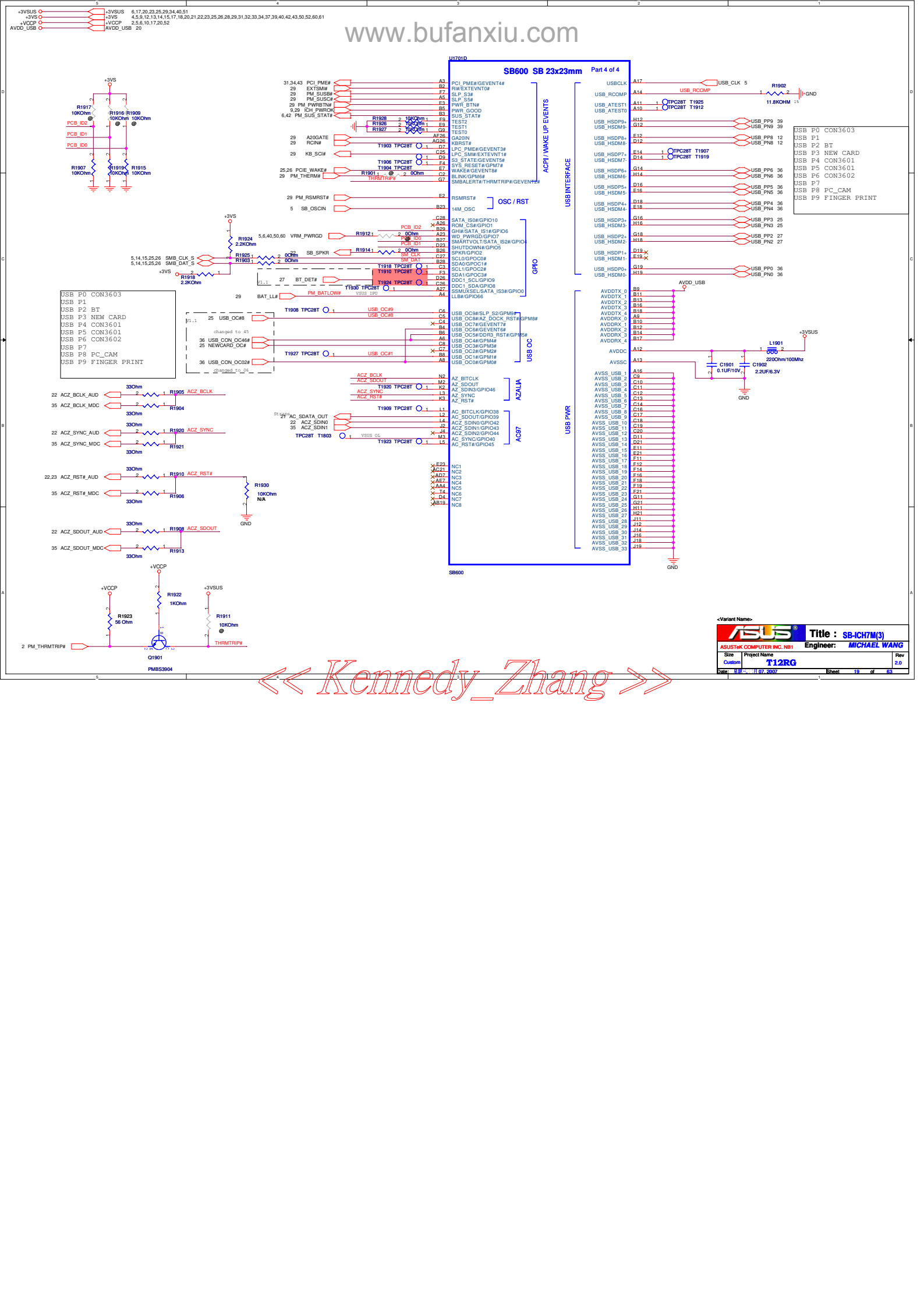
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 16 of 63	

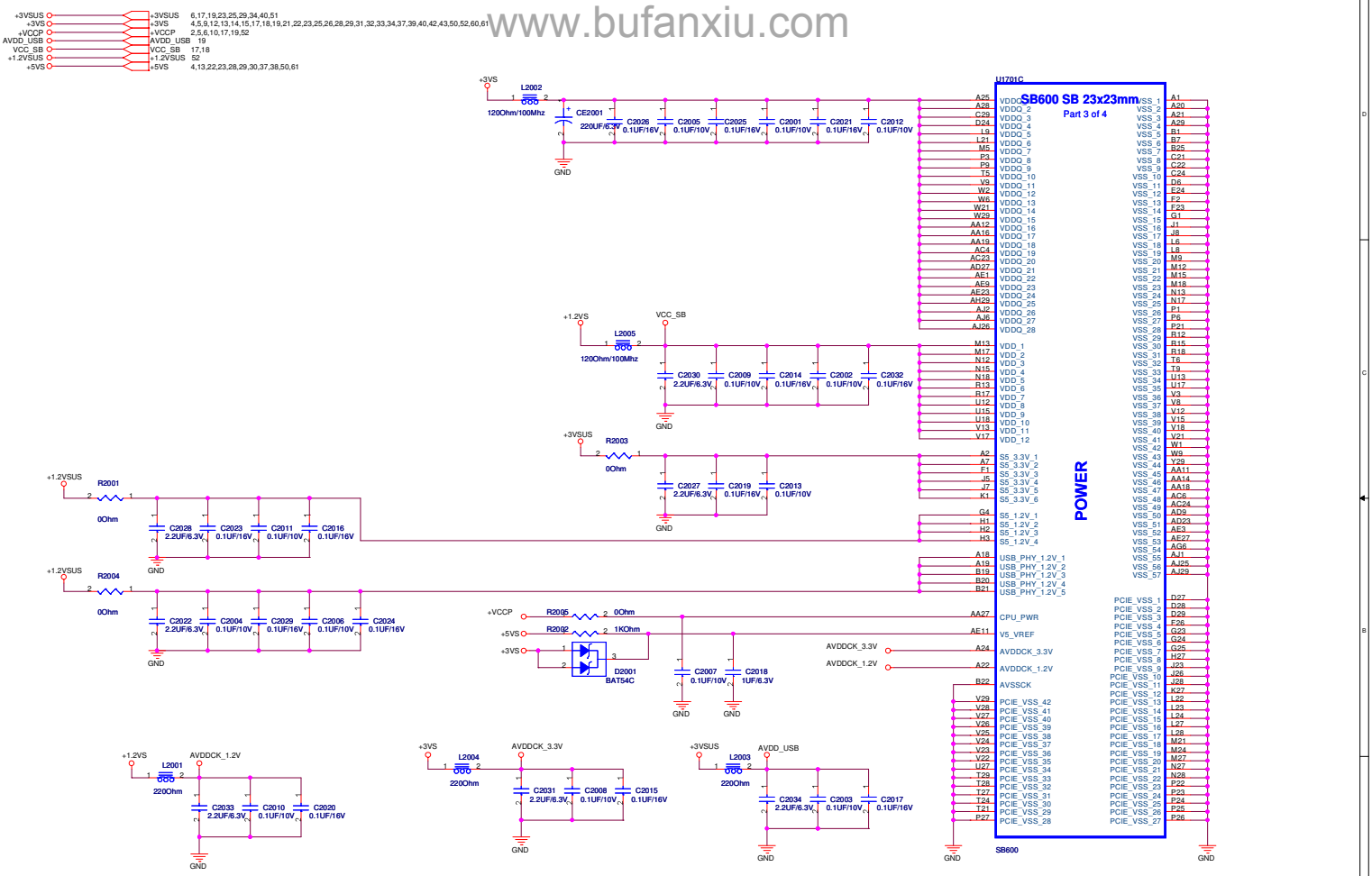

www.bufanxiu.com
SB600 SB 23x23mm
Part 1 of 4
U1701A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
LPC
CPU
RTC
XTAL
SB600
Mount 0 ohm
(ATI confirmed)
FOLLOW RTC LAYOUT
GUIDE ON THIS
Follow T12F
Manual power on
To Power circuits
<< Kennedy_Zhang >>
Title : SB-ICH7-M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: MICHAEL WANG
Project Name T12RG
Rev 2.0
Sheet 17 of 63



<Variant Name>

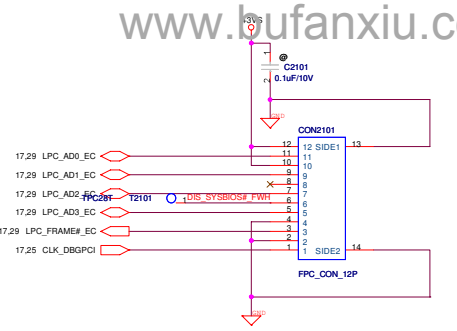
ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 18 of 63	

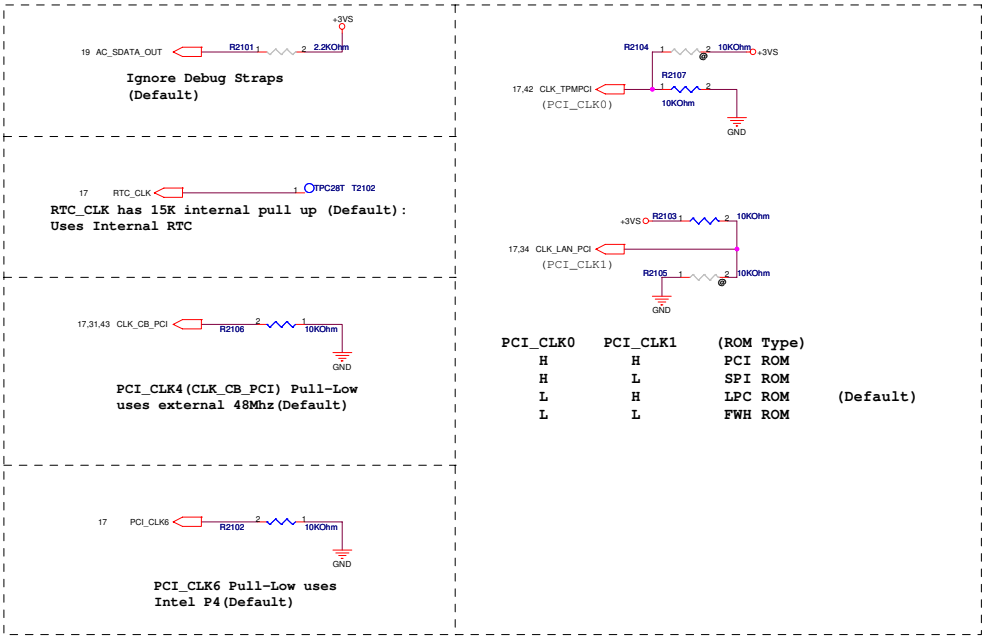




<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(PWR)		
	Engineer: MICHAEL WANG		
Size: Custom	Project Name: T12RG		Rev: 2.0
Date: 星期二, 三月 07, 2007		Sheet 20 of 63	





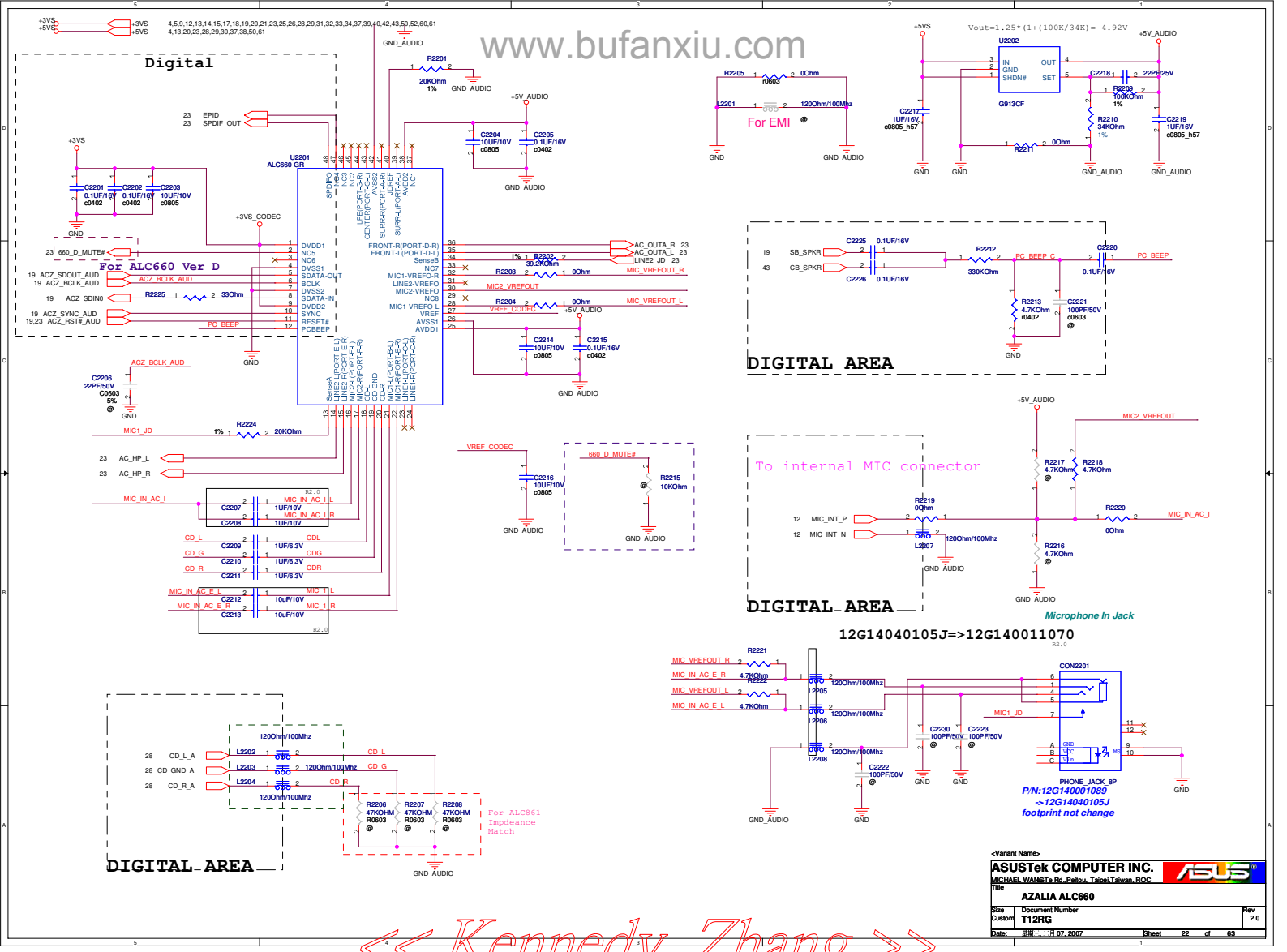
<Variant Name>

Title : BLOCK DIAGRAM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 21 of 63



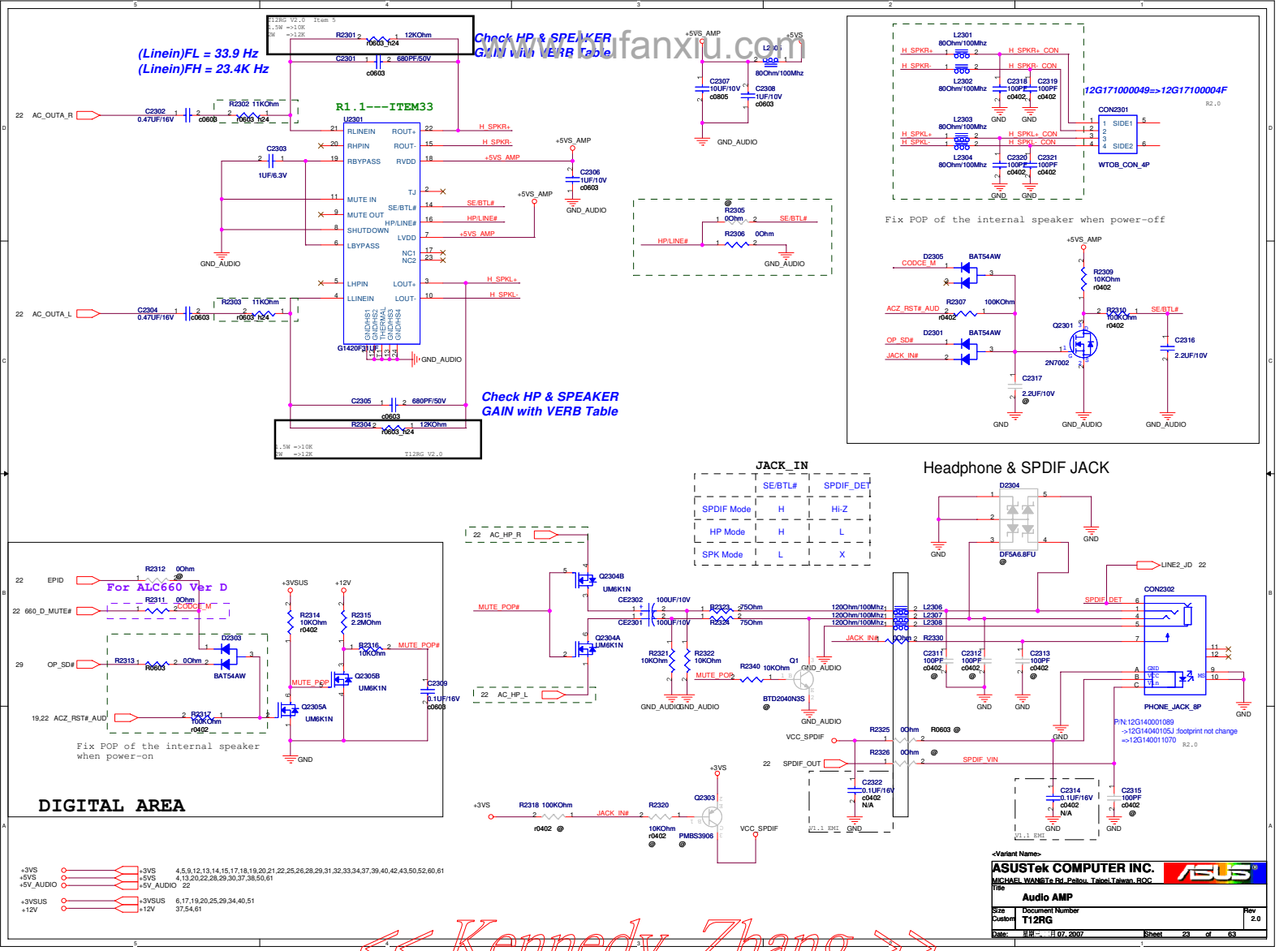
<Variant Name>

ASUSTek COMPUTER INC.
MICHAEL WANGTe Rd. Peitou, Taipei,Taiwan, ROC

Title: AZALIA ALC660

Size	Document Number	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 22 of 63



<Variant Name>

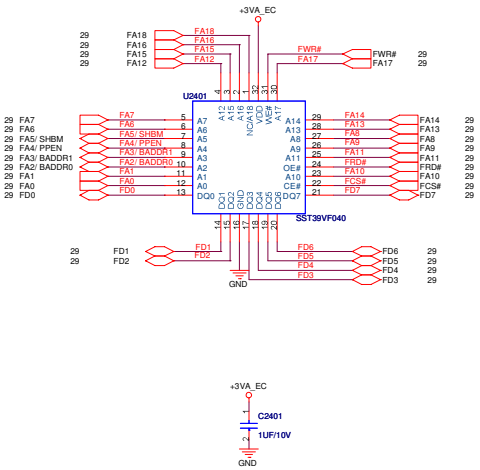
ASUSTek COMPUTER INC.
MICHAEL WANG Te Rd. Peitou, Taipei,Taiwan, ROC

Title	Audio AMP	
Size: Custom	Document Number: T12RG	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 23 of 63	

+3VA_EC +3VA_EC 26,29

ISA ROM

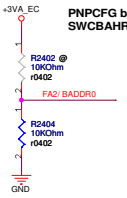
0.01A

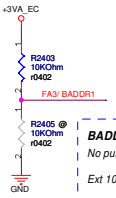


EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

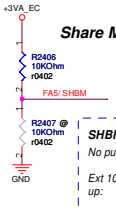




BADDR[1:0]

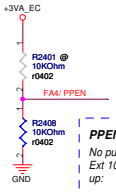
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

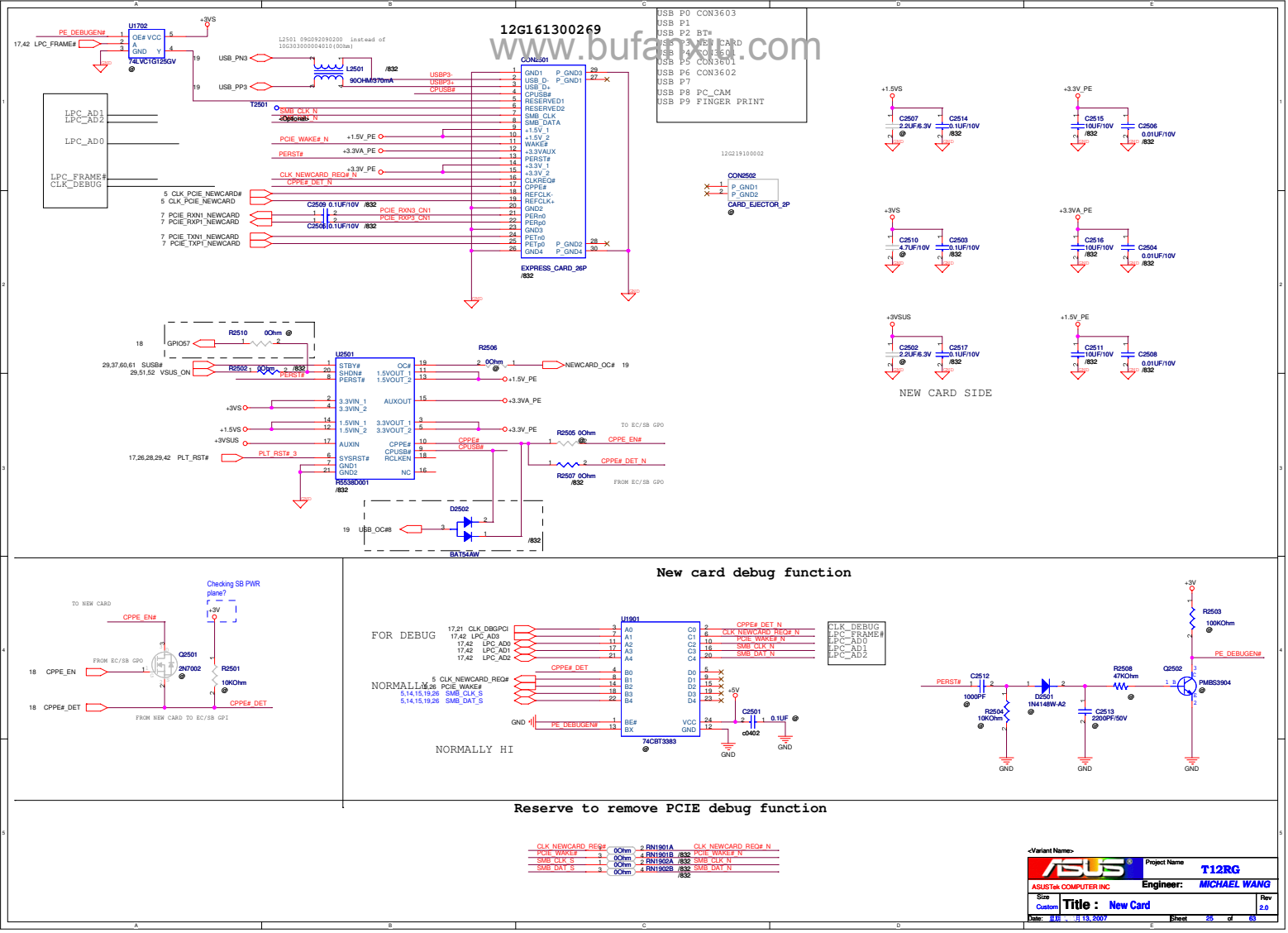


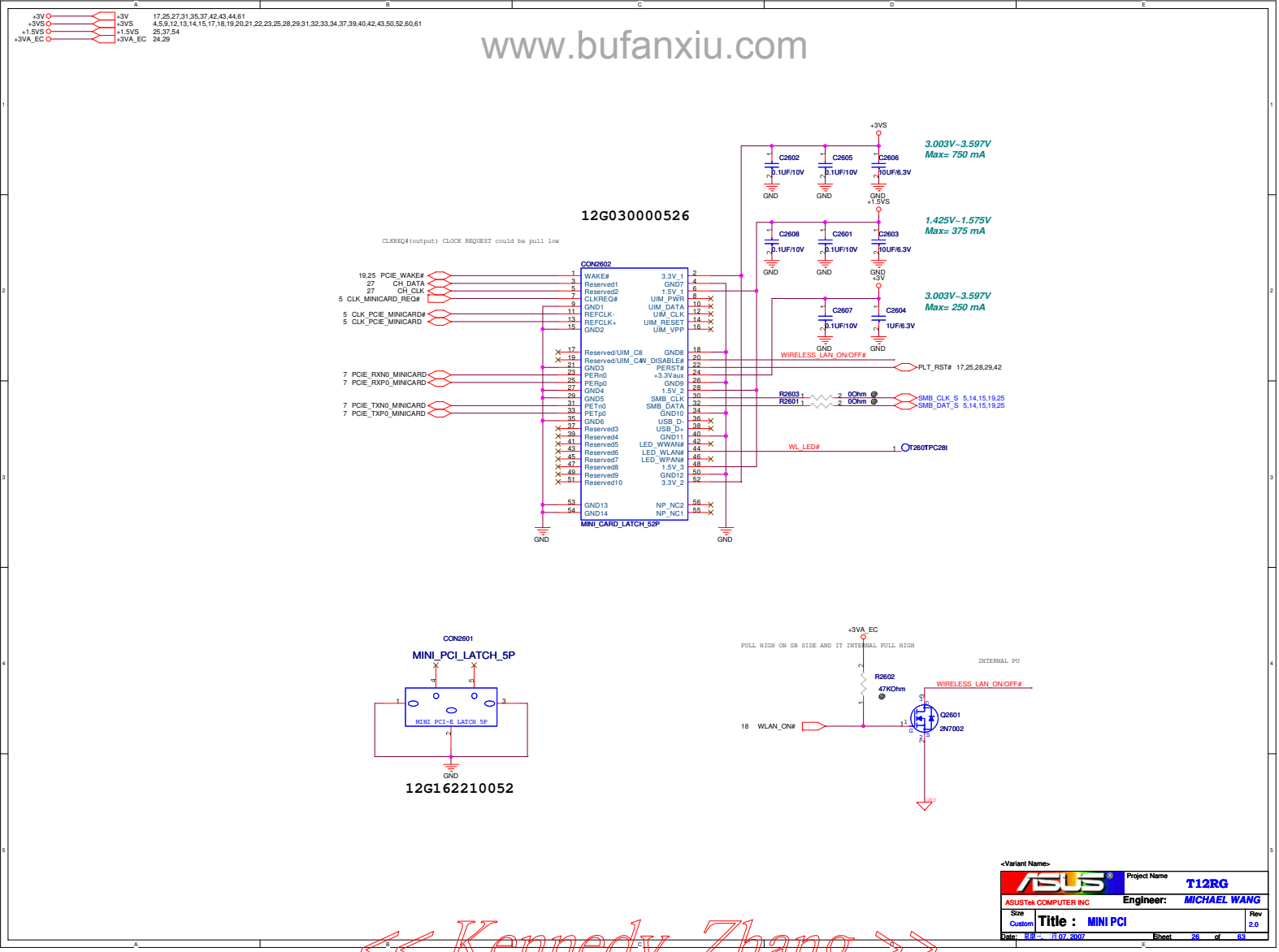
PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 十一月 07, 2007	Sheet 24 of 63	





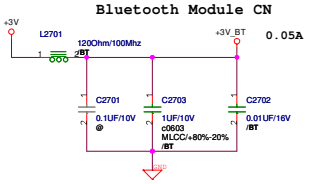
<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : MINI PCI	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 26 of 63	

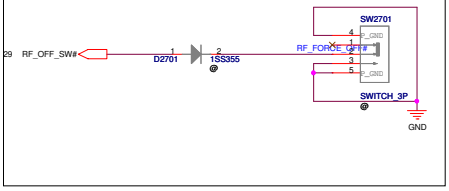
+3V +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

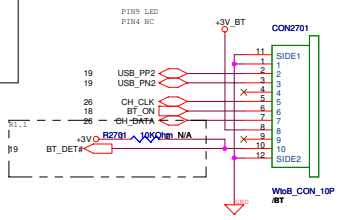
Bluetooth Module CN



RESERVED RF SWITCH



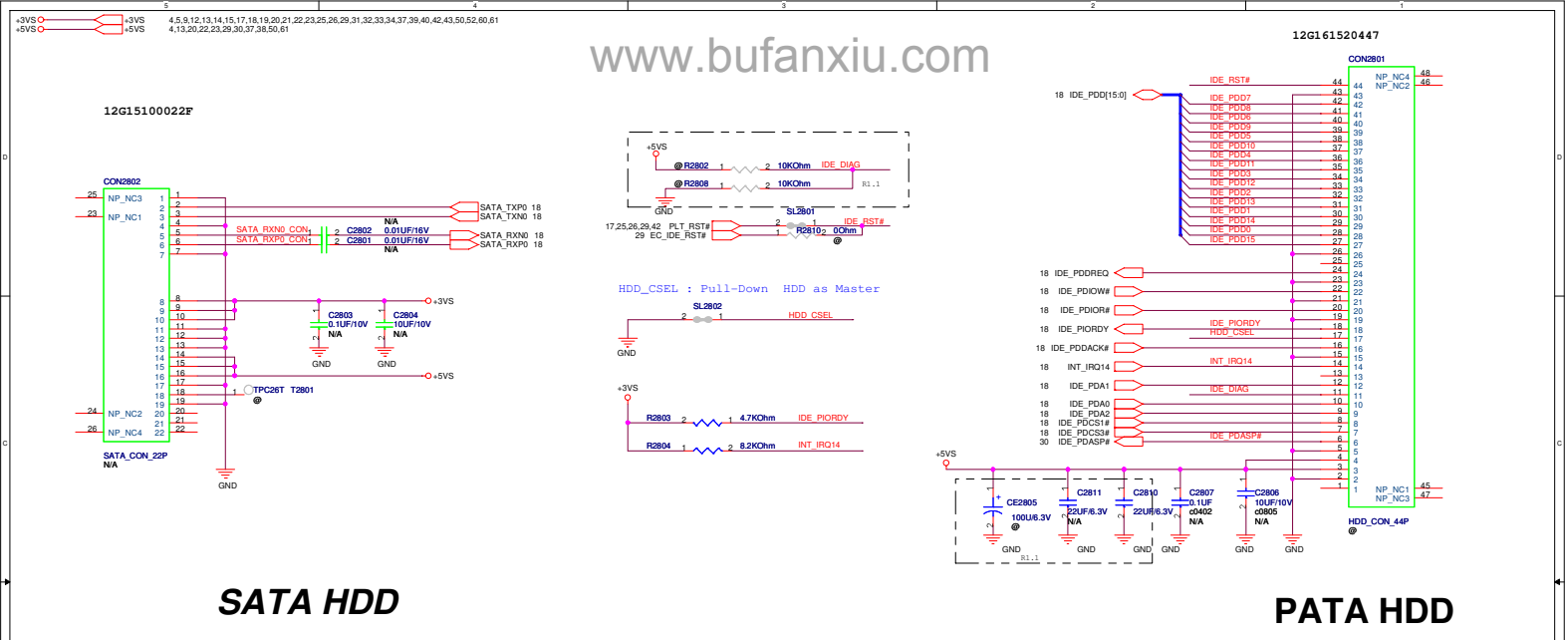
12G17101010L



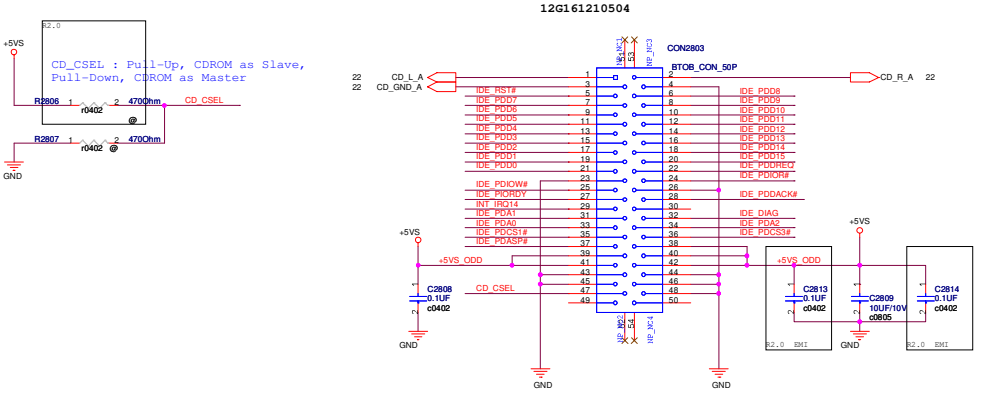

```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT
```

<Variant Name>

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 27 of 63	

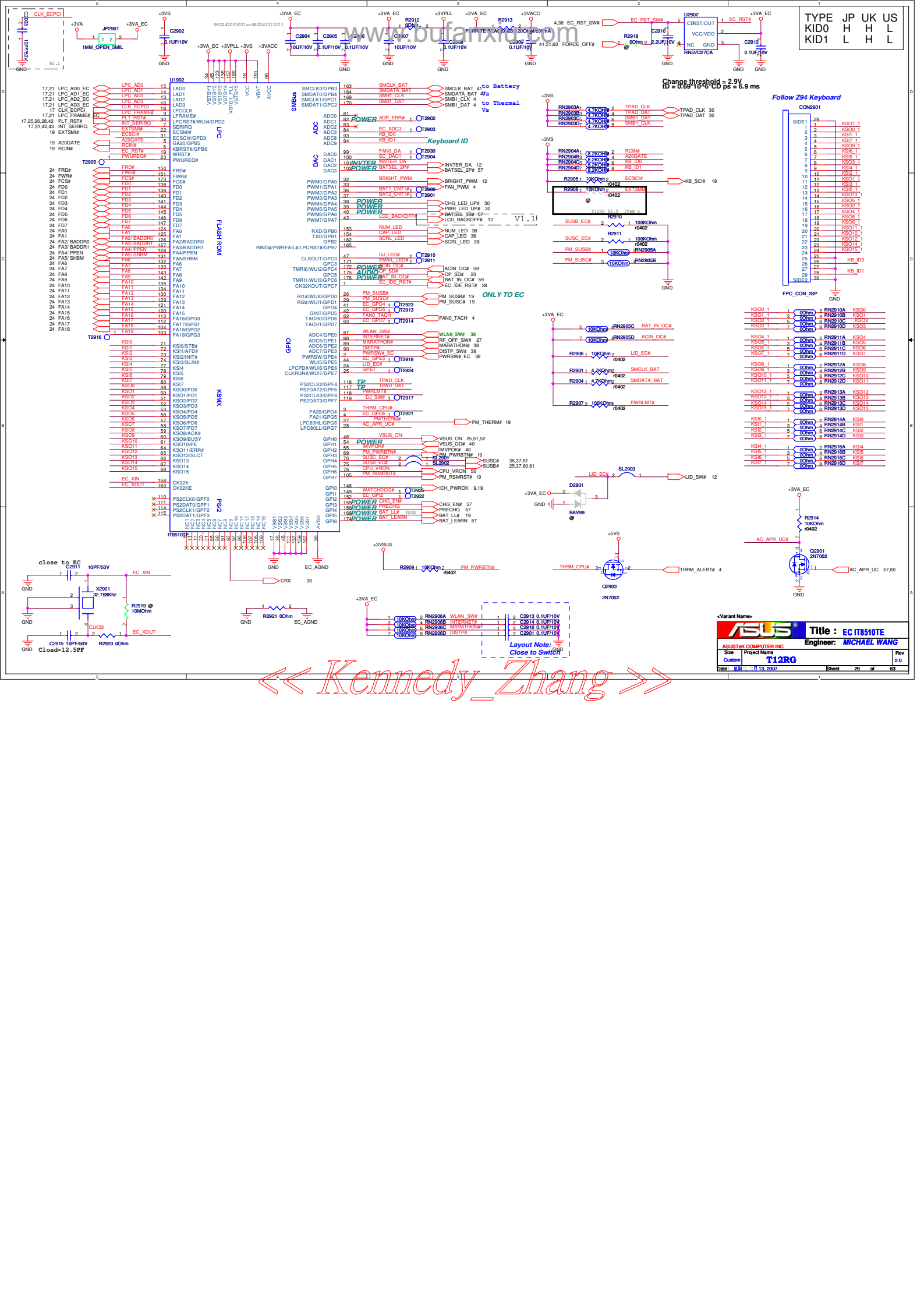


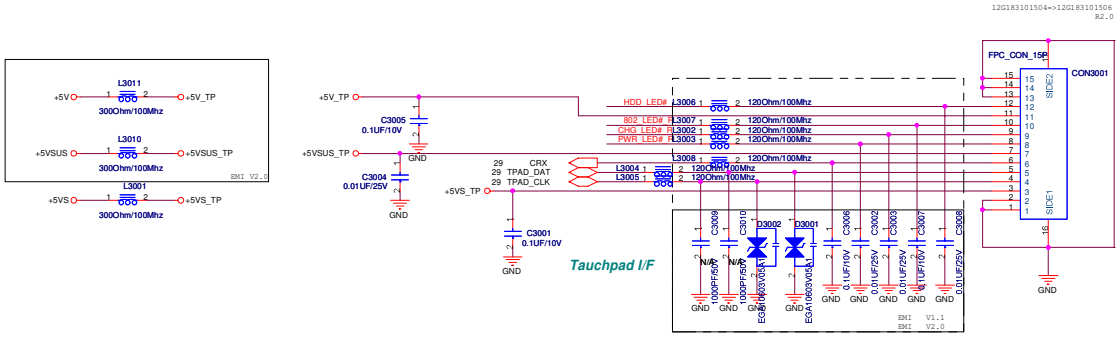
CD-ROM



<Variant Name>

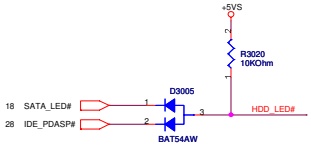
ASUSTeK COMPUTER INC. NB1	Title : PATA-SATA & ODD	
	Engineer:	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 28 of 63	


TYPE JP UK US
KID0 H H L
KID1 L H L
www.bufanxin.com
U1902
IT8510TE
JP2901
1MM_OPEN_SMIL
U2902
RN5VD27CA
T2905
T2916
CON2901
FPC_CON_28P
Follow Z94 Keyboard
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
to Battery Va
to Thermal Vs
Keyboard ID
ONLY TO EC
Layout Note:
Close to Switch
close to EC
Cload=12.5PF
Title : EC IT8510TE
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
T12RG
Date: 13, 2007
Sheet 29 of 63
<Variant Name>
<< Kennedy_Zhang >>

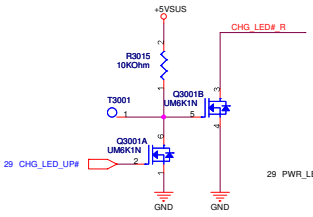


Touchpad

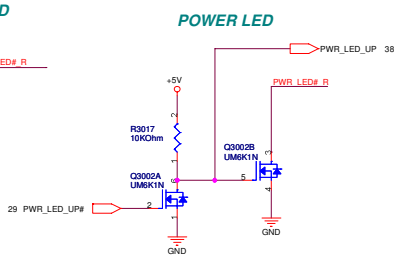
HDD LED



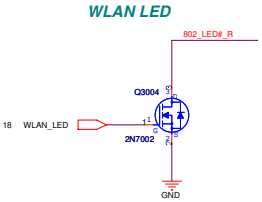
CHARGE LED



POWER LED



WLAN LED



<Variant Name>

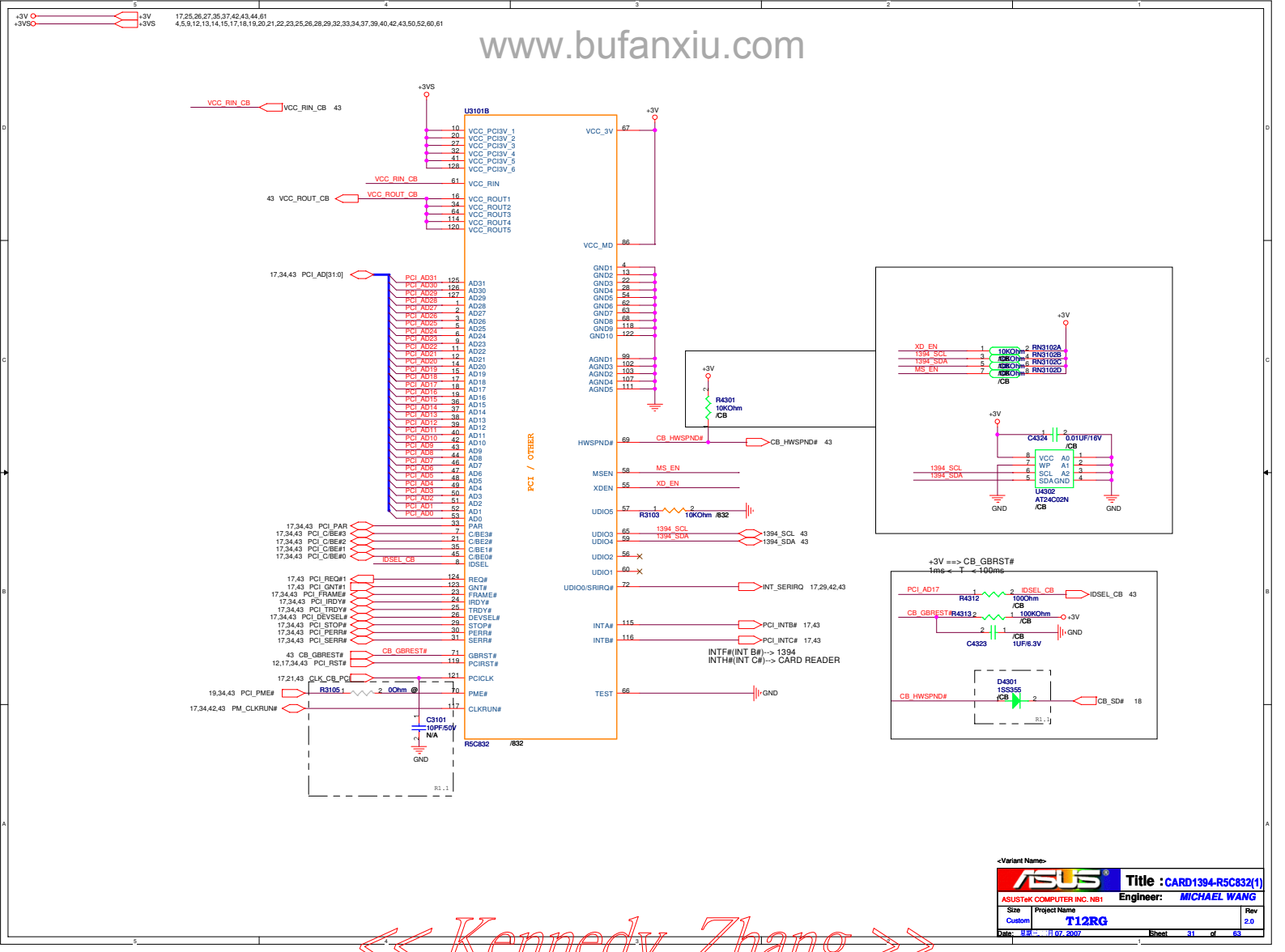
ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: MICHAEL WANG

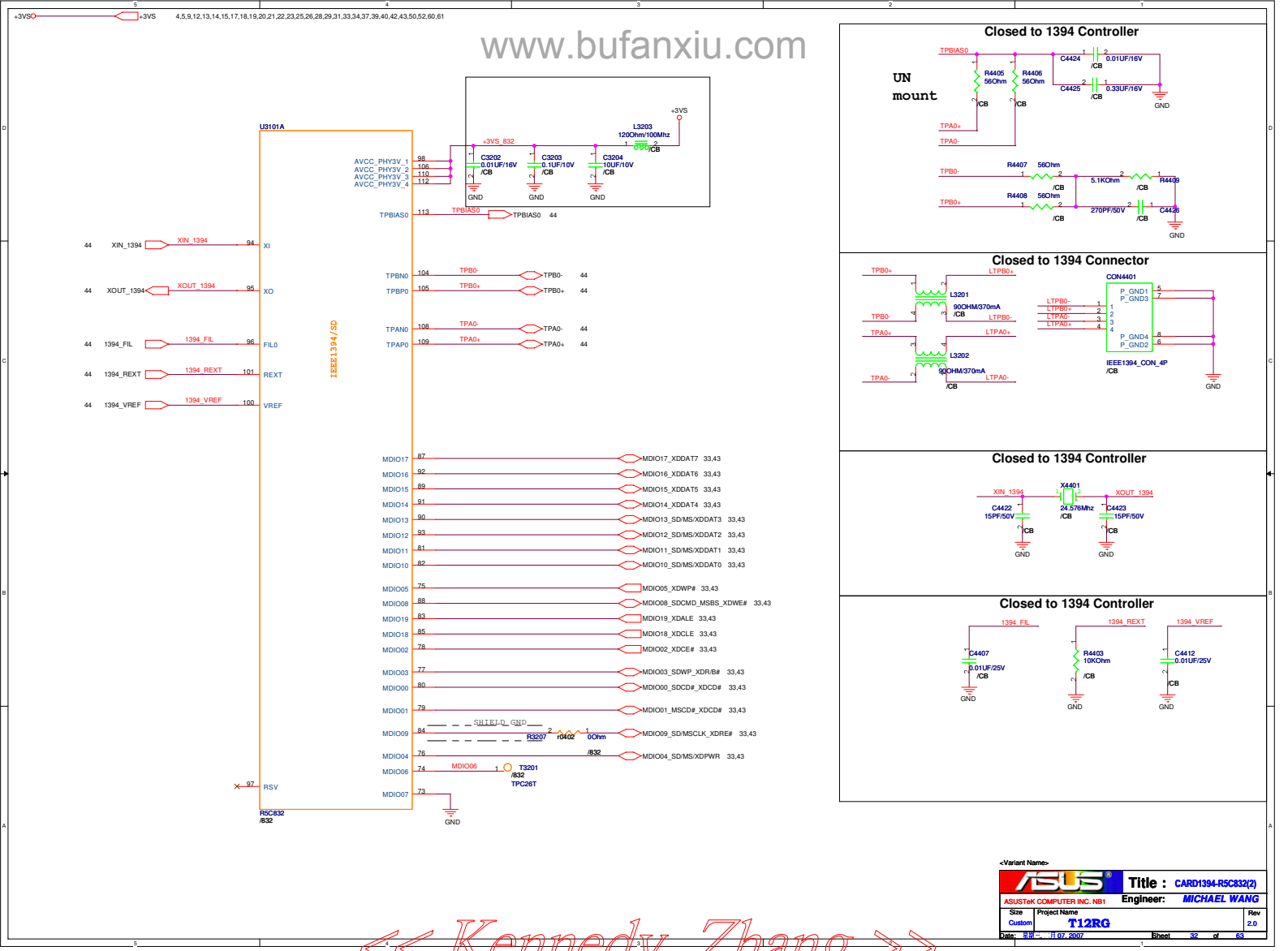
Size	Project Name	Rev
A3	T12RG	2.0

Date: 星期一, 月 07, 2007 Sheet 30 of 63



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(1)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 31 of 63	



Closed to 1394 Controller

UN mount

Closed to 1394 Connector

Closed to 1394 Controller

Closed to 1394 Controller

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 32 of 63	

Name	Drive	Name	Drive
MDIO00	I – PU	MDIO10	I/O – PU
MDIO01	I – PU	MDIO11	I/O – PU
MDIO02	O – PU	MDIO12	I/O – PU
MDIO03	I – PU	MDIO13	I/O – PU
MDIO04	O – 3V	MDIO14	I/O – PU
MDIO05	O – 3V	MDIO15	I/O – PU
MDIO06	O – 3V	MDIO16	I/O – PU
MDIO07	I – 3V	MDIO17	I/O – PU
MDIO08	I/O – PU	MDIO18	I/O – PU
MDIO09	I/O – PU	MDIO19	I/O – PU

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD WP/xD/LE control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

SD/MMC/MS/MS-PRO Card Reader Socket

32,43 MDIO17_XDDAT7 — MDIO17_XDDAT7
32,43 MDIO16_XDDAT6 — MDIO16_XDDAT6
32,43 MDIO15_XDDAT5 — MDIO15_XDDAT5
32,43 MDIO14_XDDAT4 — MDIO14_XDDAT4
32,43 MDIO13_SD/MS/XDDAT3 — MDIO13_SD/MS/XDDAT3
32,43 MDIO12_SD/MS/XDDAT2 — MDIO12_SD/MS/XDDAT2
32,43 MDIO11_SD/MS/XDDAT1 — MDIO11_SD/MS/XDDAT1
32,43 MDIO10_SD/MS/XDDAT0 — MDIO10_SD/MS/XDDAT0

32,43 MDIO05_XDWP# — MDIO05_XDWP#
32,43 MDIO08_SDCMD_MSBS_XDWE# — MDIO08_SDCMD_MSBS_XDWE#
32,43 MDIO19_XDALE — MDIO19_XDALE
32,43 MDIO18_XDCLE — MDIO18_XDCLE
32,43 MDIO02_XDCE# — MDIO02_XDCE#

32,43 MDIO03_SDWP_XDR/B# — MDIO03_SDWP_XDR/B#
32,43 MDIO00_SDCD#_XDCD# — MDIO00_SDCD#_XDCD#
32,43 MDIO01_MSCD#_XDCD# — MDIO01_MSCD#_XDCD#
32,43 MDIO09_SD/MSCLK_XDRE# — MDIO09_SD/MSCLK_XDRE#

12G340004402

+VCCCA
C3304 270P @
CON3301 CARD_READER_44P /CB

1	MS_GND1	XD_CD	23
2	MS_BS	XD_GND1	24
3	MS_DATA1	XD_R/B	25
4	MS_DATA0	XD_RE	26
5	MS_DATA2	XD_CE	27
6	MS_INS	XD_CLE	28
7	MS_DATA3	XD_ALE	29
8	MS_SCLK	XD_WE	30
9	MS_VCC	XD_WP	31
10	MS_GND2	XD_GND2	32
11	SD_DAT2	XD_D0	33
12	SD_DAT3	XD_D1	34
13	SD_CMD	XD_D2	35
14	SD_GND1	XD_D3	36
15	SD_VCC	XD_D4	37
16	SD_CLK	XD_D5	38
17	SD_GND2	XD_D6	39
18	NC1	XD_D7	40
19	SD_DAT0	XD_VCC	41
20	SD_DAT1	NC2	42
21	SD_CD_SW	SD_WP_SW	43
22	SD_CD_COM	SD_WP_COM	44
45	NP_NC1	NP_NC2	46
47	GND1	GND2	48

MDIO08_SDCMD_MSBS_XDWE#
MDIO11_SD/MS/XDDAT1
MDIO10_SD/MS/XDDAT0
MDIO12_SD/MS/XDDAT2
MSCD#
MDIO13_SD/MS/XDDAT3
MDIO09_SD/MSCLK_XDRE#
SD_DAT2
MDIO13_SD/MS/XDDAT3
MDIO08_SDCMD_MSBS_XDWE#
MDIO09_SD/MSCLK_XDRE#
MDIO10_SD/MS/XDDAT0
SD_DAT1
SDCD#
XD_CD#
MDIO03_SDWP_XDR/B#
MDIO09_SD/MSCLK_XDRE#
MDIO02_XDCE#
MDIO18_XDCLE
MDIO19_XDALE
MDIO08_SDCMD_MSBS_XDWE#
MDIO05_XDWP#
MDIO10_SD/MS/XDDAT0
MDIO11_SD/MS/XDDAT1
MDIO12_SD/MS/XDDAT2
MDIO13_SD/MS/XDDAT3
MDIO14_XDDAT4
MDIO15_XDDAT5
MDIO16_XDDAT6
MDIO17_XDDAT7
MDIO03_SDWP_XDR/B#

+VCCCA
C3306 3300PF/50V N/A
C3305 270P @

+3VS
Q3306 IRLML5103PBF /CB
R3305 100KOhm /CB
+VCCCA
C3308 0.1UF/10V /CB
Place as close to card reader socket as possible
32,43 MDIO04_SD/MS/XDPWR

+VCCCA
C3307 0.01UF/10V @
C3309 0.01UF/10V /CB
C3310 0.01UF/10V /CB
R3306 150K /CB
C3311 2.2UF/6.3V /CB
Place as close to card reader socket as possible

To coorect the problem when MS Duo adaptor is in use.

+12VS
SDCD#
R3301 10KOhm /CB
Q3301A UM6K1N /CB
GND
MDIO11_SD/MS/XDDAT1
Q3301B UM6K1N /CB
SD_DAT1
MDIO12_SD/MS/XDDAT2
Q3302A UM6K1N /CB
SD_DAT2

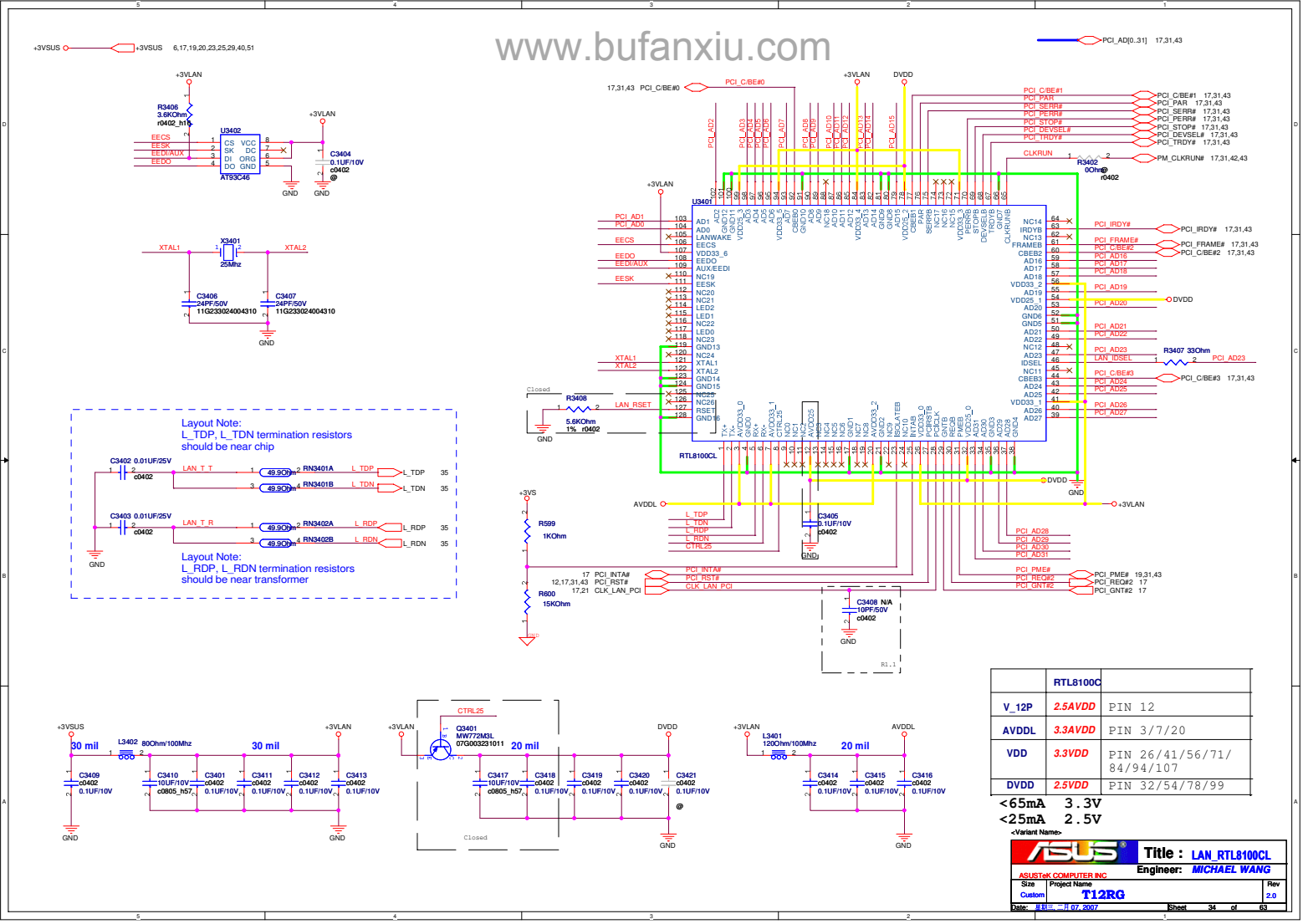
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

+3VS
R3302 10KOhm /CB
XD_CD#
SDCD#
D3301 DAP202K /CB
R3208 0Ohm r0402 @
Q3302B UM6K1N /CB
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D3302 DAP202K /CB
+3VS
R3304 10KOhm /CB
MSCD#
For Memory Stick Duo Adaptor shielding ground issue

+12VS +12VS 12,37,61
+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61

<Variant Name>

ASUSTek COMPUTER INC
Project Name: T12RG
Engineer: MICHAEL WANG
Size: Custom
Title : CardReader
Rev: 2.0
Date: 星期三, 一月 07, 2007
Sheet 33 of 63



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

<65mA 3.3V
<25mA 2.5V
<Variant Name>

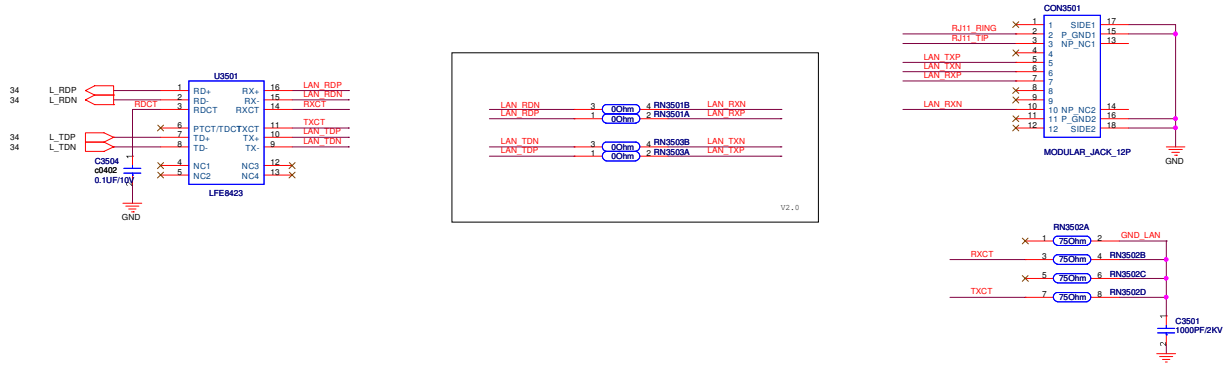
ASUSTeK COMPUTER INC
Title : LAN_RTL8100CL
Engineer: MICHAEL WANG
Size: Custom
Project Name: T12RG
Rev: 2.0
Date: 星期二 07, 2007
Sheet 34 of 63

<< Kennedy_Zhang >>

+3V +3V 17,25,26,27,31,37,42,43,44,61

LAN PORT

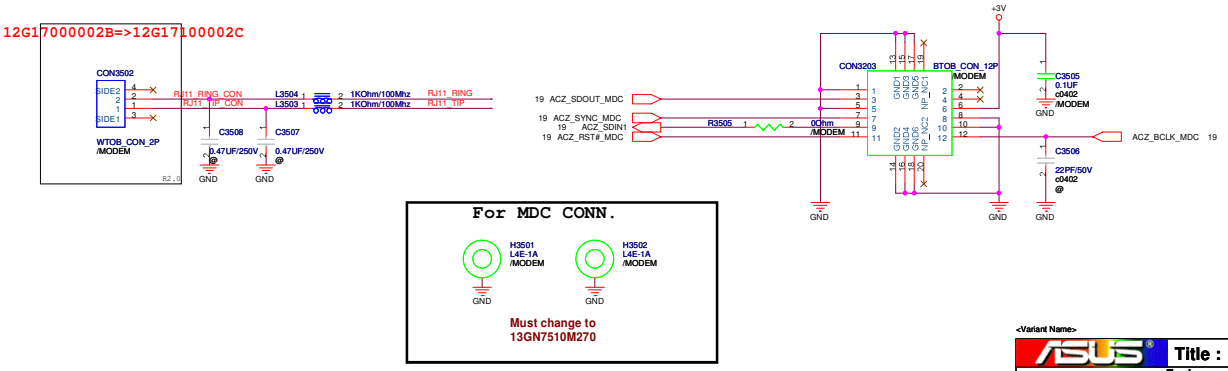
12G142111120



MDC CONNECTOR

12G161200124

12G17000002B=>12G17100002C



<Variant Name>

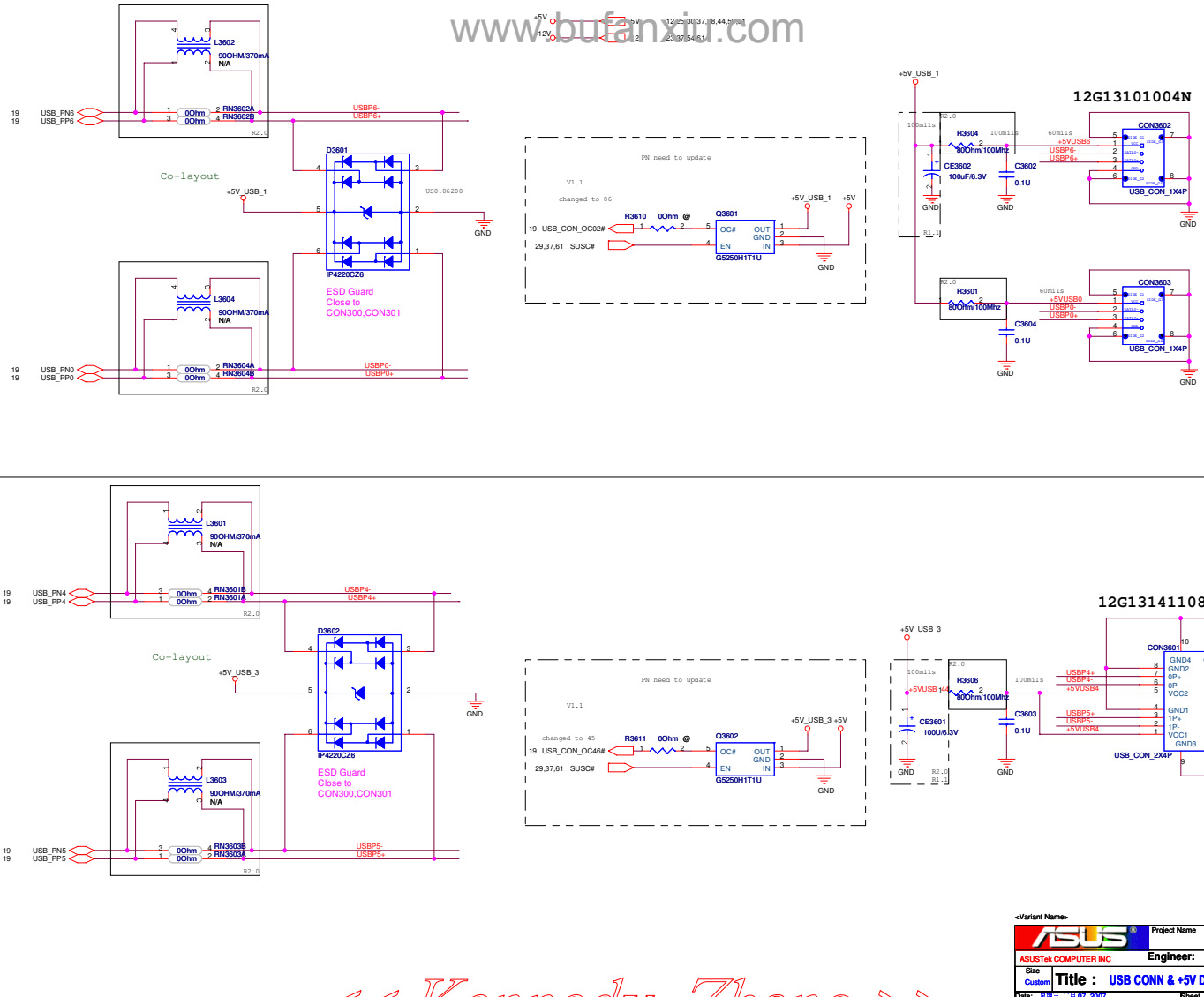
Title : RJ11/45 & MDC

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

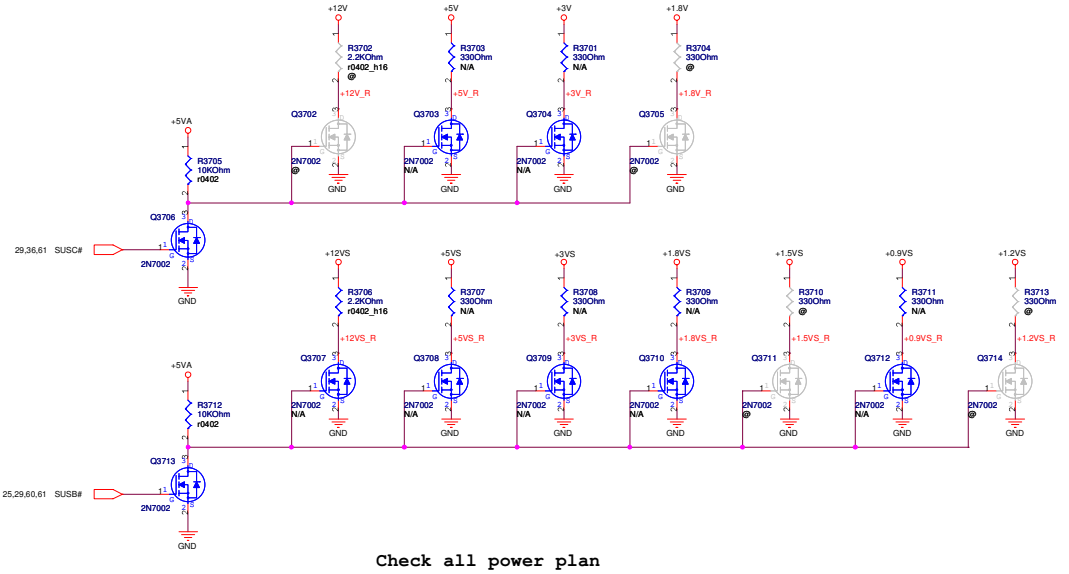
Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期三, 二月 07, 2007 Sheet 35 of 63



<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 36 of 63	

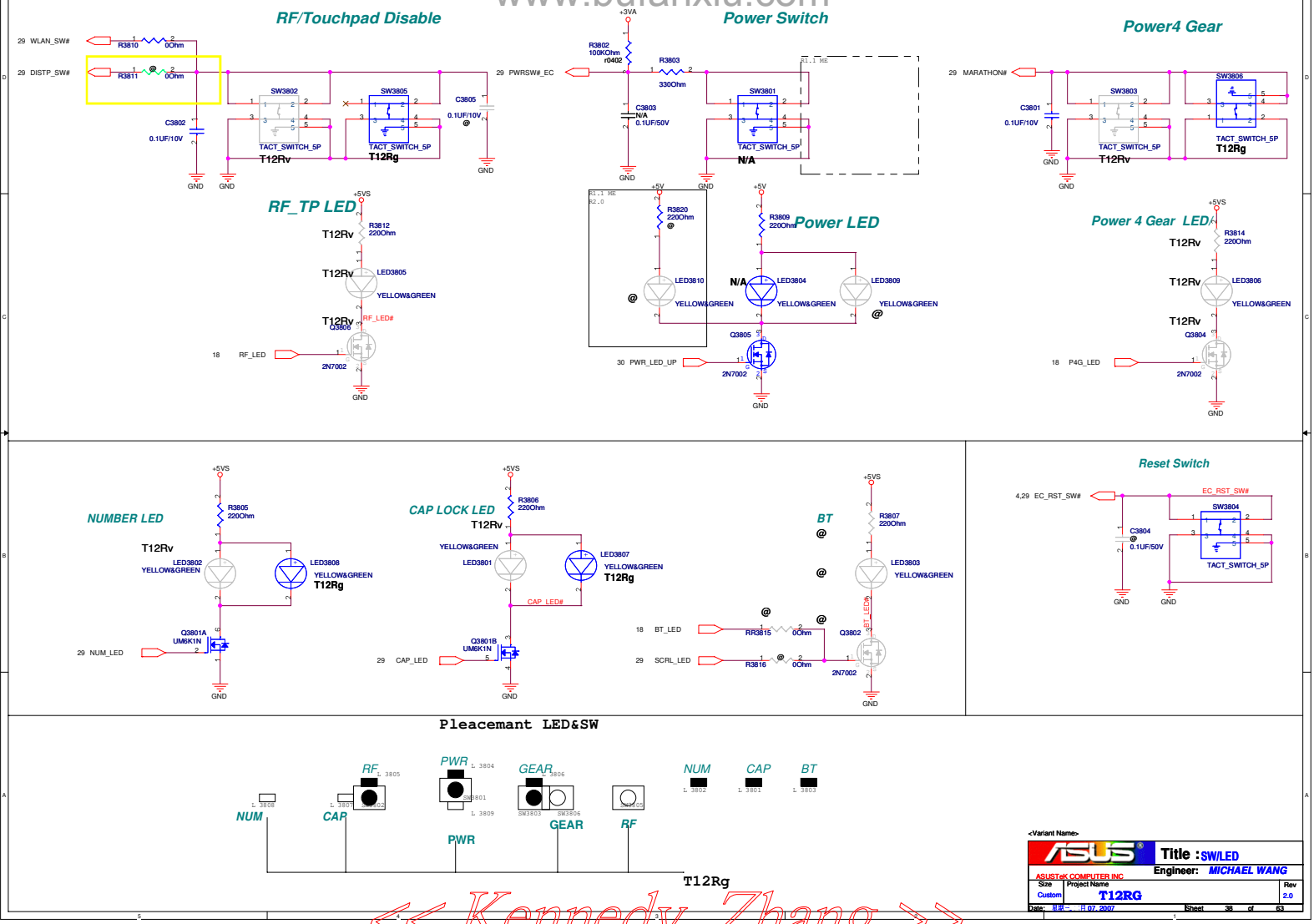


Check all power plan

<Variant Name>

ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期三, 一月 07, 2007	Sheet 37 of 63	

Main Board SW & LED



<Variant Name>

ASUSTeK COMPUTER INC

Title : SW/LED

Engineer: MICHAEL WANG

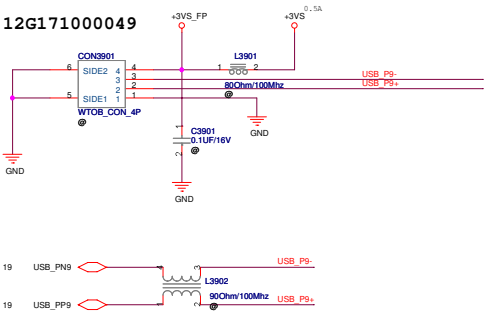
Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 月 07, 2007 Sheet 38 of 63

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT



<Variant Name>

Title : FINGER PRINT

ASUSTeK COMPUTER INC

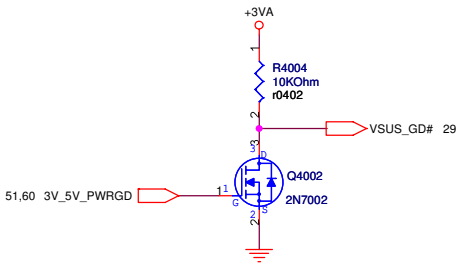
Engineer: MICHAEL WANG

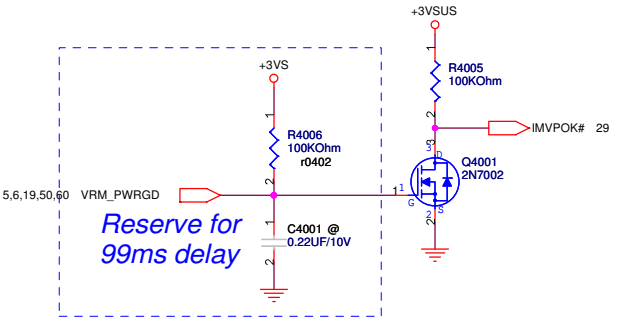
Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 39 of 63

+3VA
+3VS
+3VSUS

+3VA 12,29,38,54,57,59,63
+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,24,25,28,29,31,32,33,34,37,39,42,43,50,52,60,61
+3VSUS 6,17,19,20,23,25,29,34,51





<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER-ON SEQ.

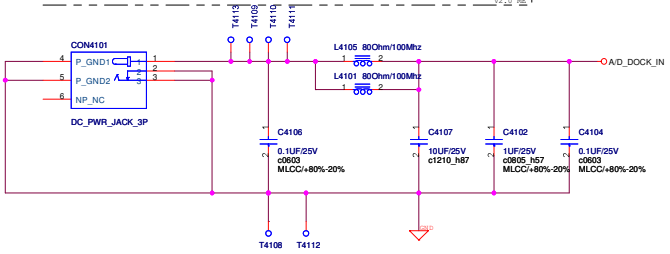
Engineer: MICHAEL WANG

Size	Project Name	Rev
A4	T12RG	2.0

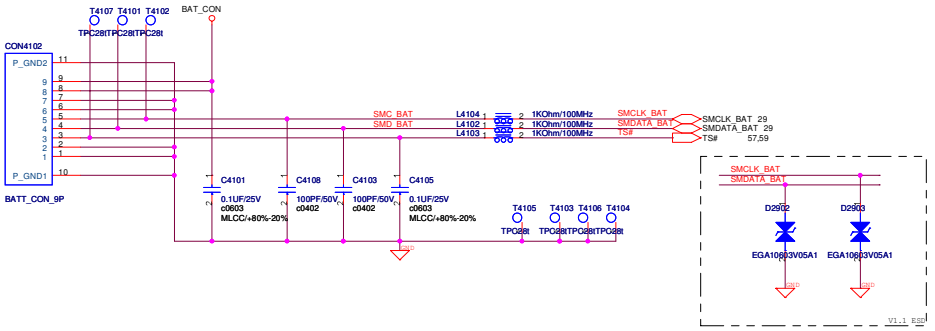
Date: 星期三, 二月 07, 2007 Sheet 40 of 63

A/D_DOCK_IN — A/D_DOCK_IN 57,59
BAT_CON — BAT_CON 57
AC_BAT_SYS — AC_BAT_SYS 12,50,51,52,53,54,57,60

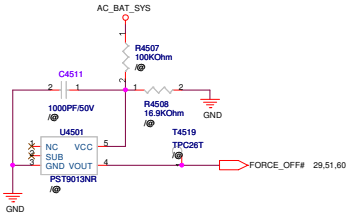
12G145002034=>12G145301038=>12G145301038Y



12G20001090G



Without Battery & Pull out Adapter
RESERVED



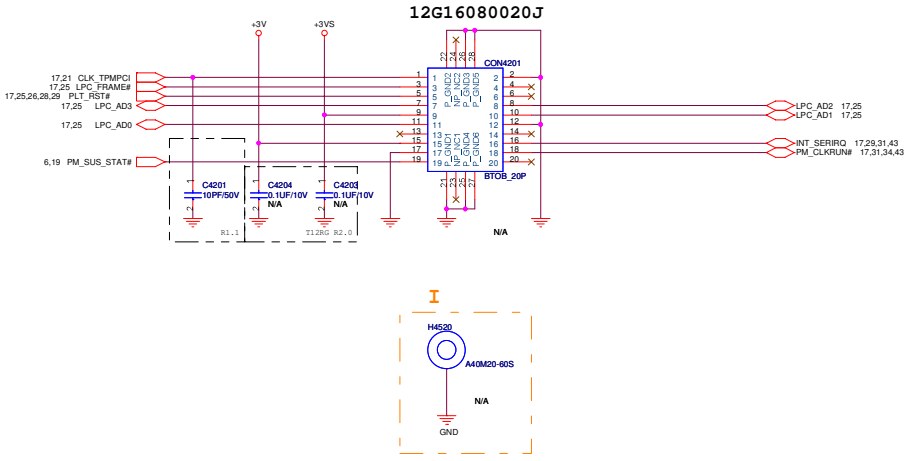
<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : DC IN	Rev: 2.0
Date: 星期二, 07, 2007	Sheet 41 of 63	

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

+3V +3V 17,25,26,27,31,35,37,43,44,61

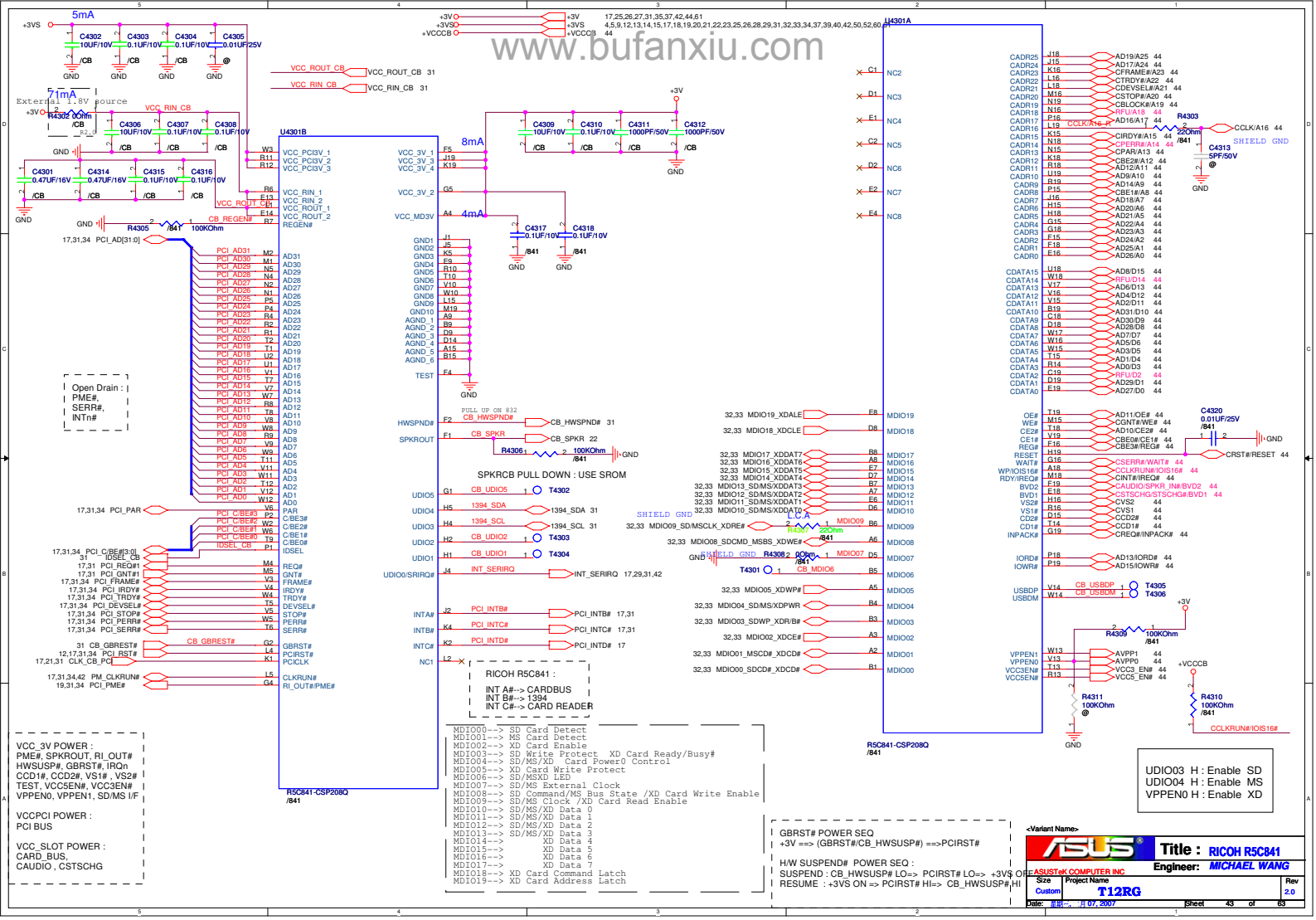
TPM Module CON
RESERVED

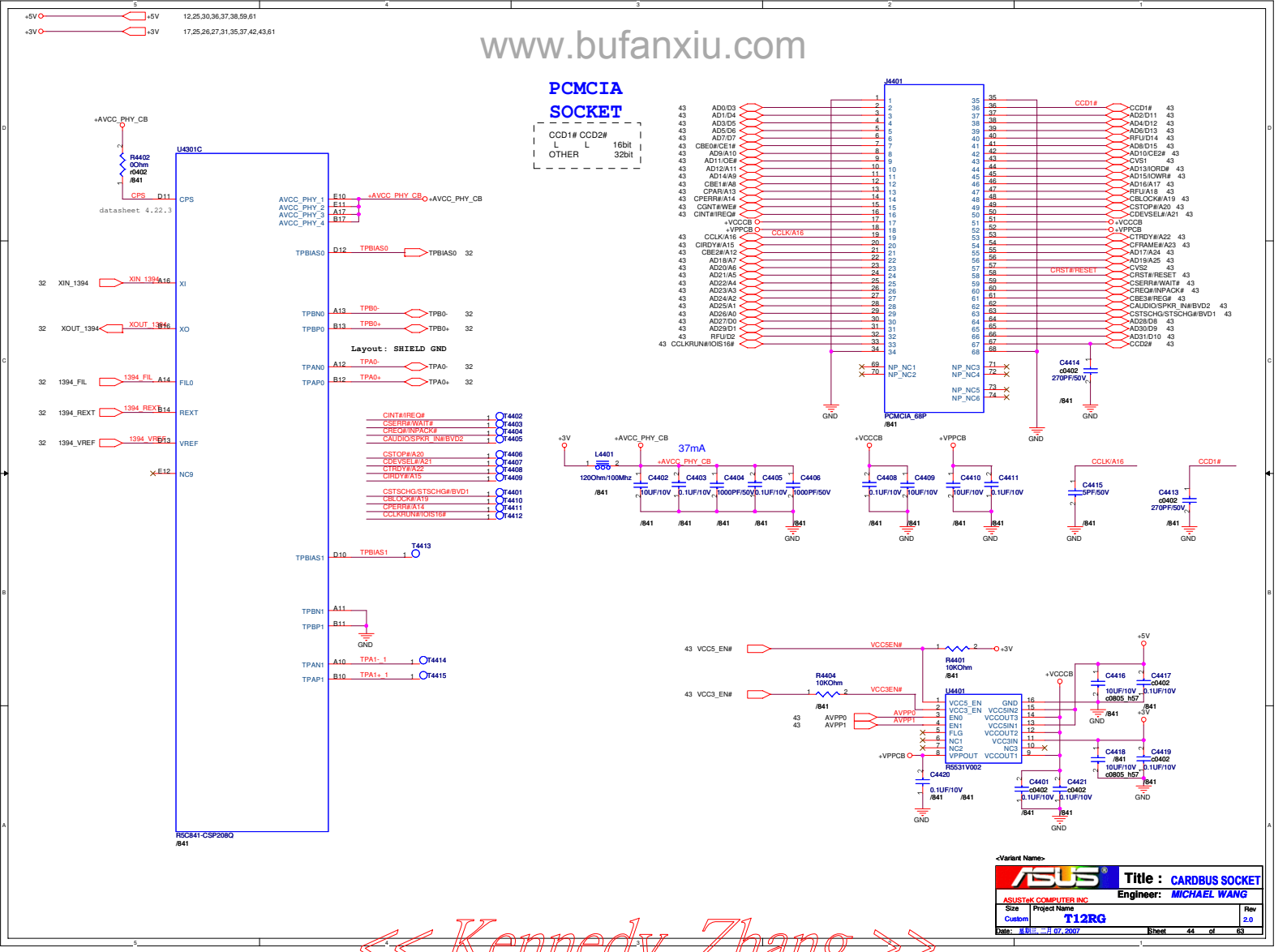


For TPM CONN.

<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 42 of 63	





<Variant Name>

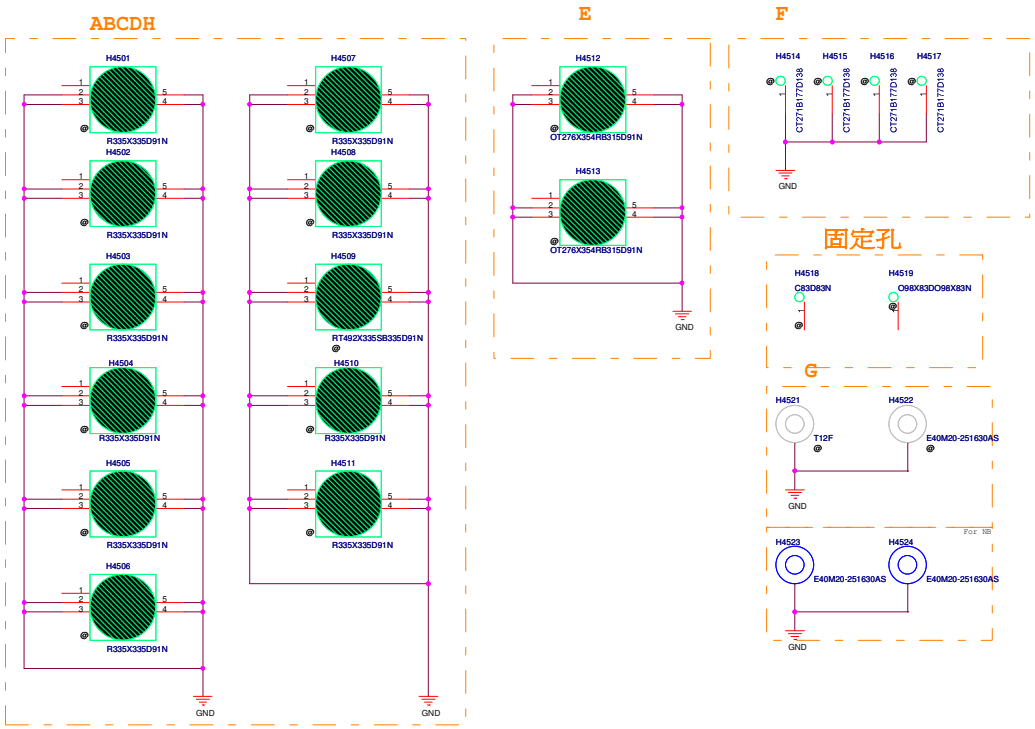
ASUSTeK COMPUTER INC

Title : CARDBUS SOCKET

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期三, 二月 07, 2007 Sheet 44 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期三, 一月 07, 2007	Sheet 45 of 63	

<Variant Name>

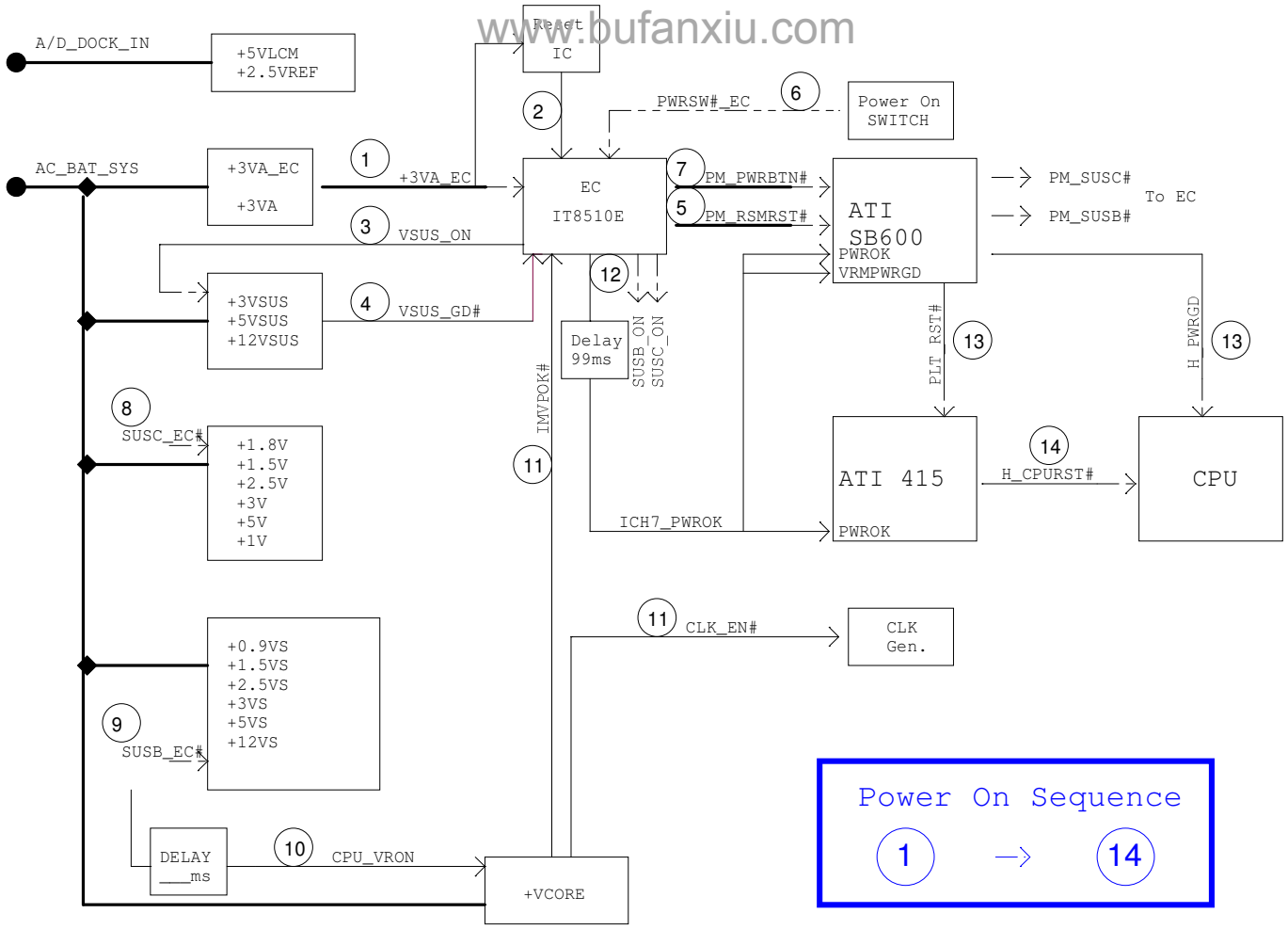
Title : HISTORY

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 46 of 63



<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 47 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB16	GPIO00/BM_BUSY#	INT_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

Title : GPIO Setting

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: [illegible] 07, 2007 Sheet 48 of 63

T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9.All PCI clock added 6.8 pF to decrease skew.
10.PWM connected to EC and back-light connected to NB
11.D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12.page 19, added BT_DET# to detect BT.
13.Page 19, adjust USB OC ping to correspond USB port
14.Page 25, modification NEW CARD debug circuit to correspond new debug card
15.page 28, we used correctly capacity for customer request.
16.page 36, we used LDO with over current protect IC
17.page 41, DC in connector add 2nd source.

ME modify
1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加螺絲鎖付記號

6.DDR2 added 2nd source
P/N :12G025022004
DDR2 DIMM 200P,1.8V,H:4mm,STD
FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.連版圖修改

T12R V2.0 Modify History

1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 10U with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006~3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

T12Rg V1.0 modify from T12R V2.0

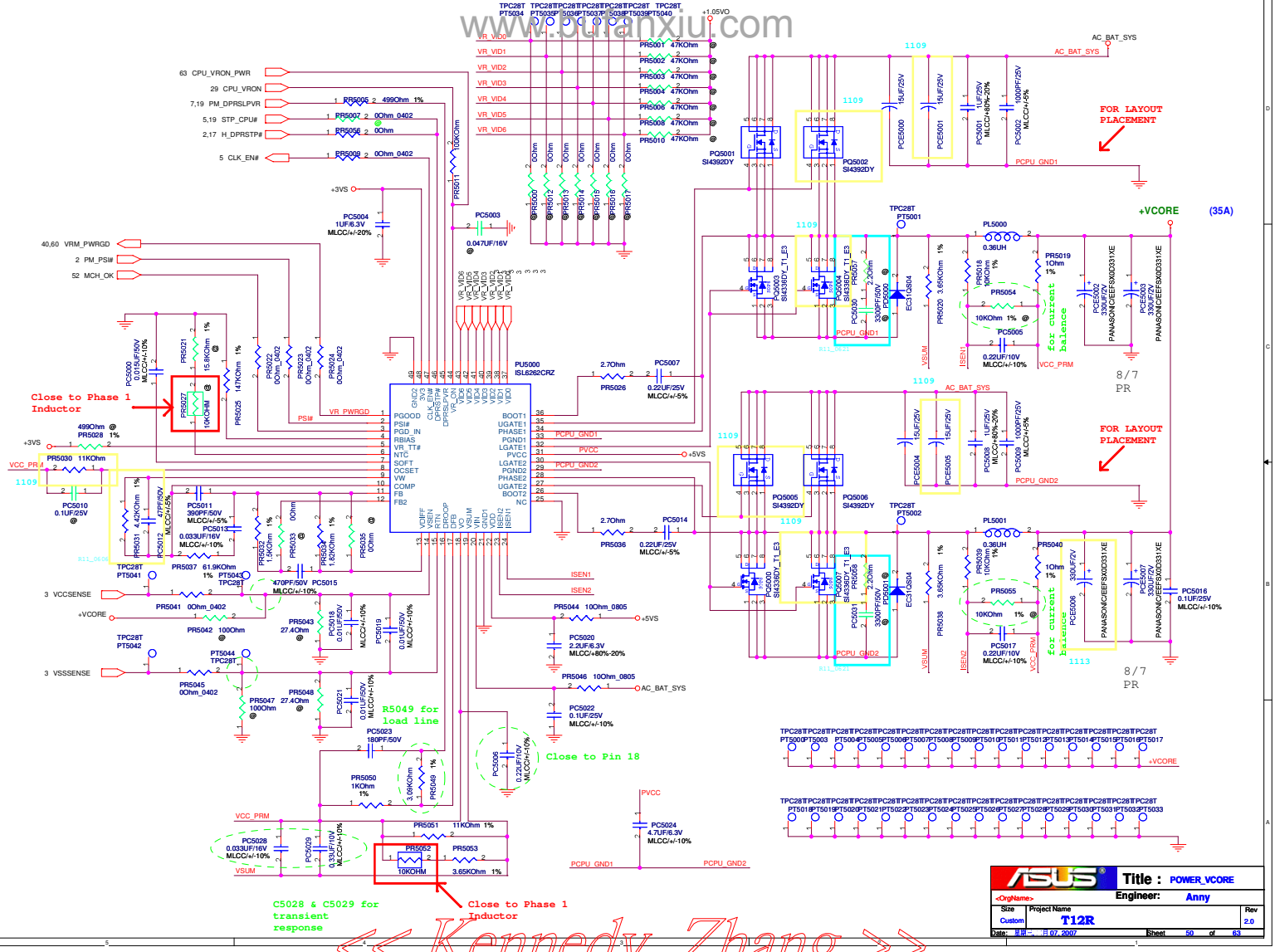
1. To modify BOM include LED(color&placement), SW(placement), HDD(PATA TO SATA), PCCAM(unmount) internal MIC(unmount) and R5C841(added 1394 cardreader and PCMCIA).

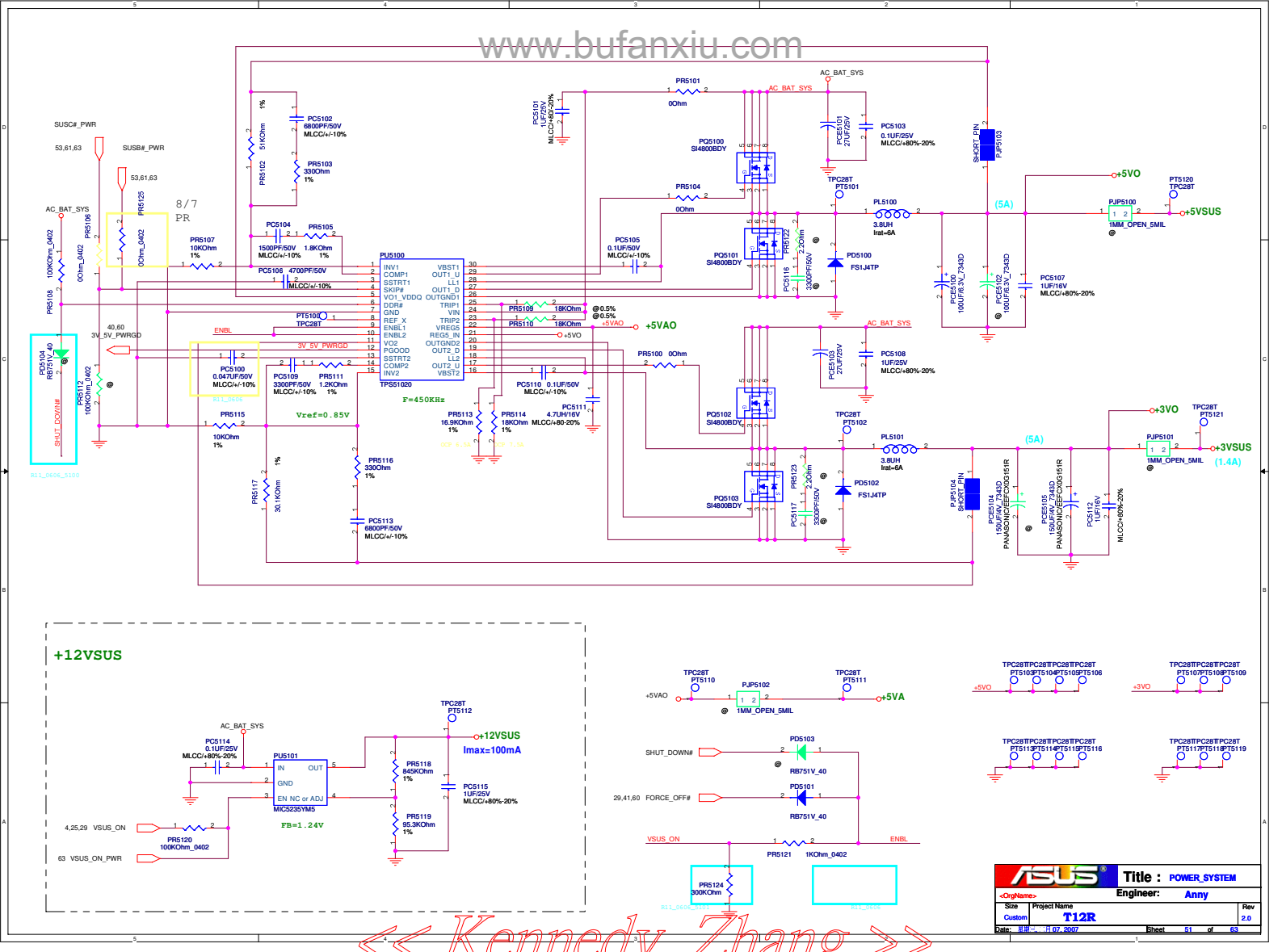
T12Rg V2.0

1. Page 12, L1203 0 Ohm to bead, EMI request.
2. Page 12, L1204 and L1205 0 Ohm to bead and mount C1222 C1223, EMI request.
3. Page 12, mount L1214 L1215 Ohm for added internal speaker.
4. Page 12, mount L1206, EMI request.
5. Page 6, R2301 and R2304 10K to 12K for 2W speaker..
6. Page 6, modify BOM, unmount R2908.

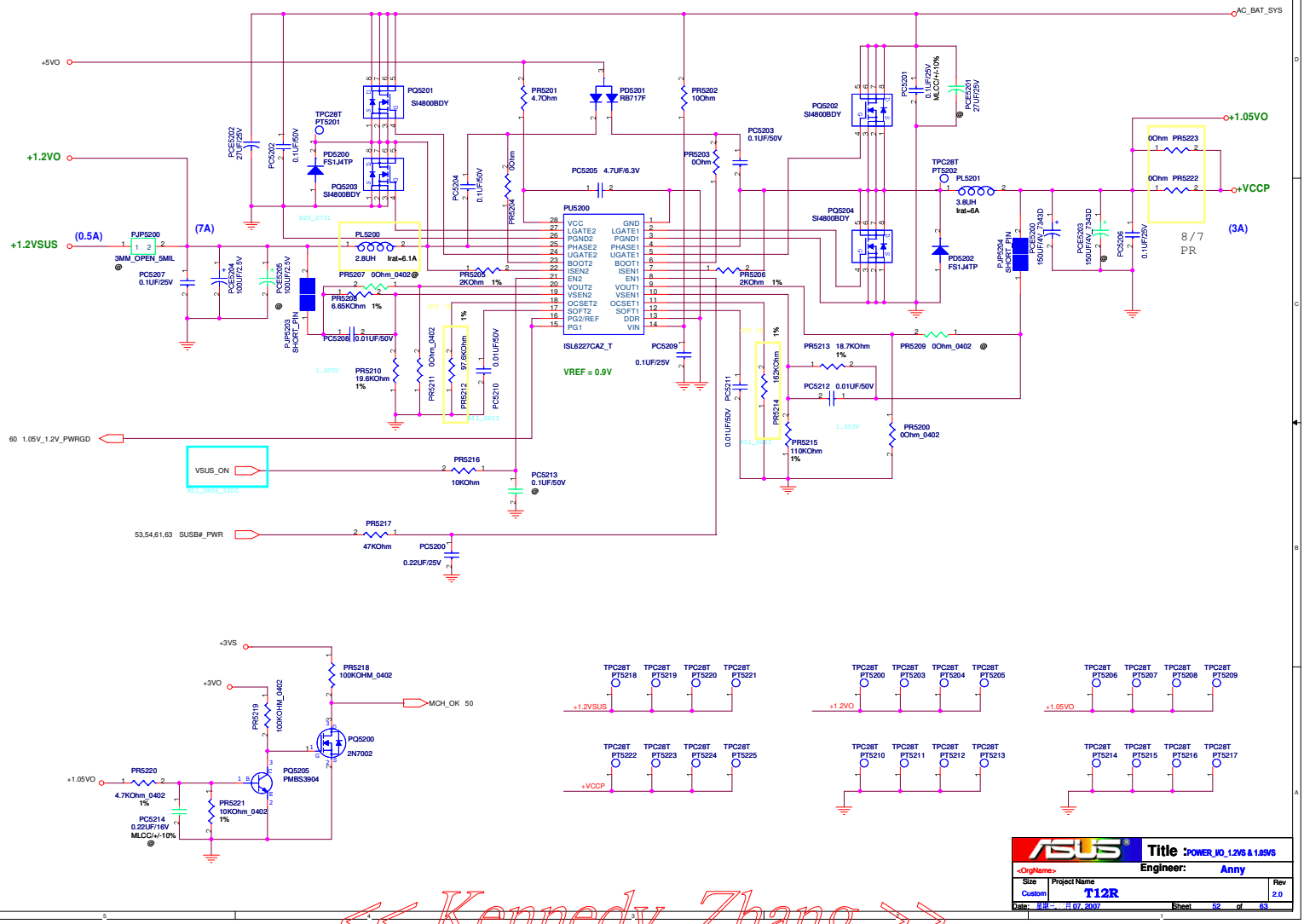
	X51 PCB X51	T12RG PCB T12R	T12RG PCB T12R	T12Rv 2.0 PCB T12R	T12Rv 2.1 PCB X51
NB	415ME	415ME	415ME	415MD	415ME
SB	SB600 A21	SB600 A21	SB600 A21	SB600 A13	SB600 A21
AUDIO	660VD	660VD	660VD	660VD	
SPDIF	N/A	N/A	N/A	N/A	
R5C832	N/A	N/A	N/A	N/A	
R5C841	OK	OK	OK	N/A	
1394	N/A	OK	OK	N/A	
CARD READER	OK	OK	OK	N/A	
PCMCIA	OK	OK	OK	N/A	
NEW CARD	N/A	N/A	N/A	N/A	
TPM	N/A	OK	OK	N/A	
BT	OK	N/A	N/A	N/A	
PC_CAM	N/A	N/A	N/A	OK	
INT. MIC.	N/A	OK	OK	OK	
MODEN	OK	N/A	OK	N/A	
TV	N/A	N/A	N/A	N/A	
SPEAKER	1.5W	2W	2W	1.5W	

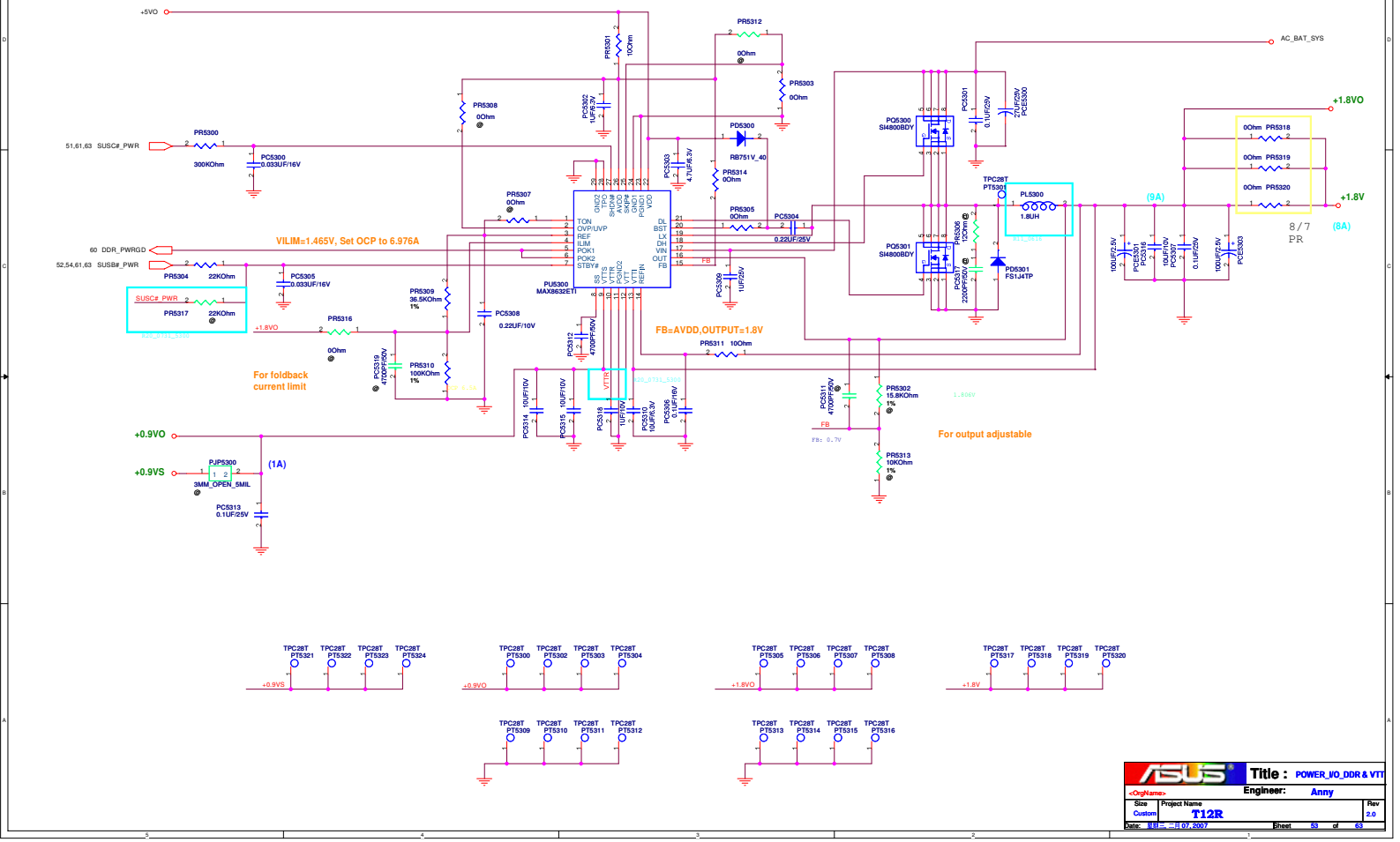
Title : HISTORY
Engineer:
Project Name: T12RG



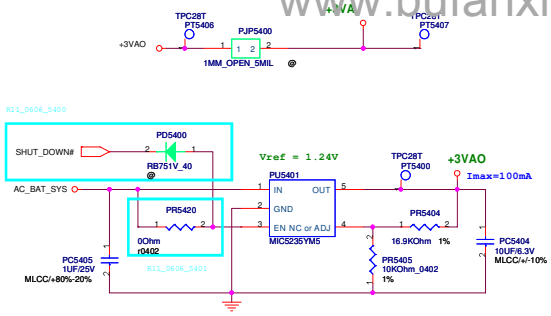


Title : POWER_SYSTEM			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 51 of 63		

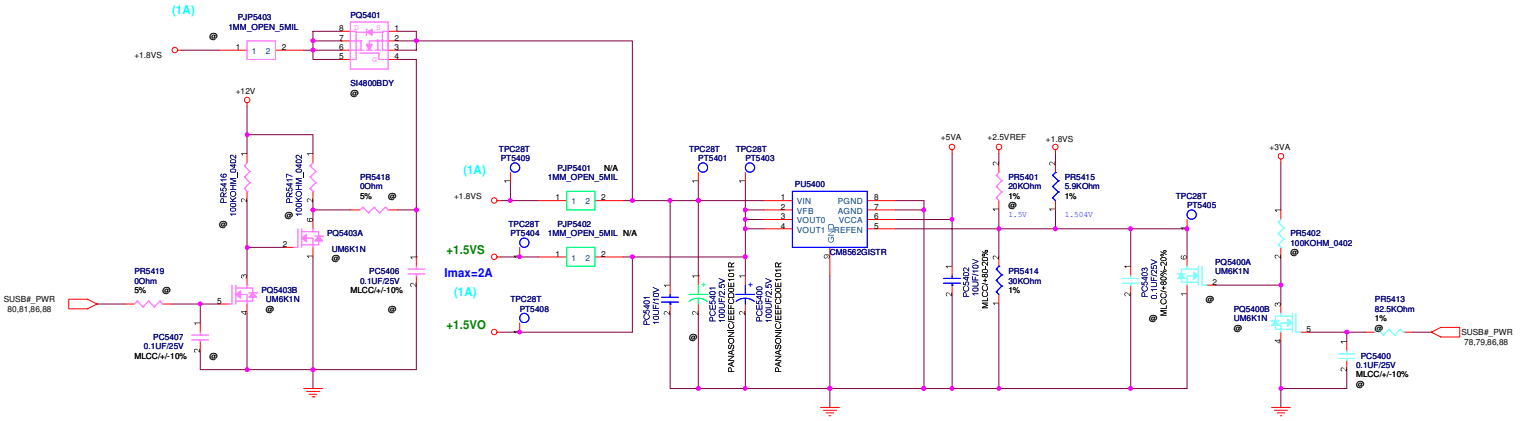




+3VAO



+2.5VS



ASUS

Title : POWER_I/O_+3VA & +2.5V

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12R	2.0

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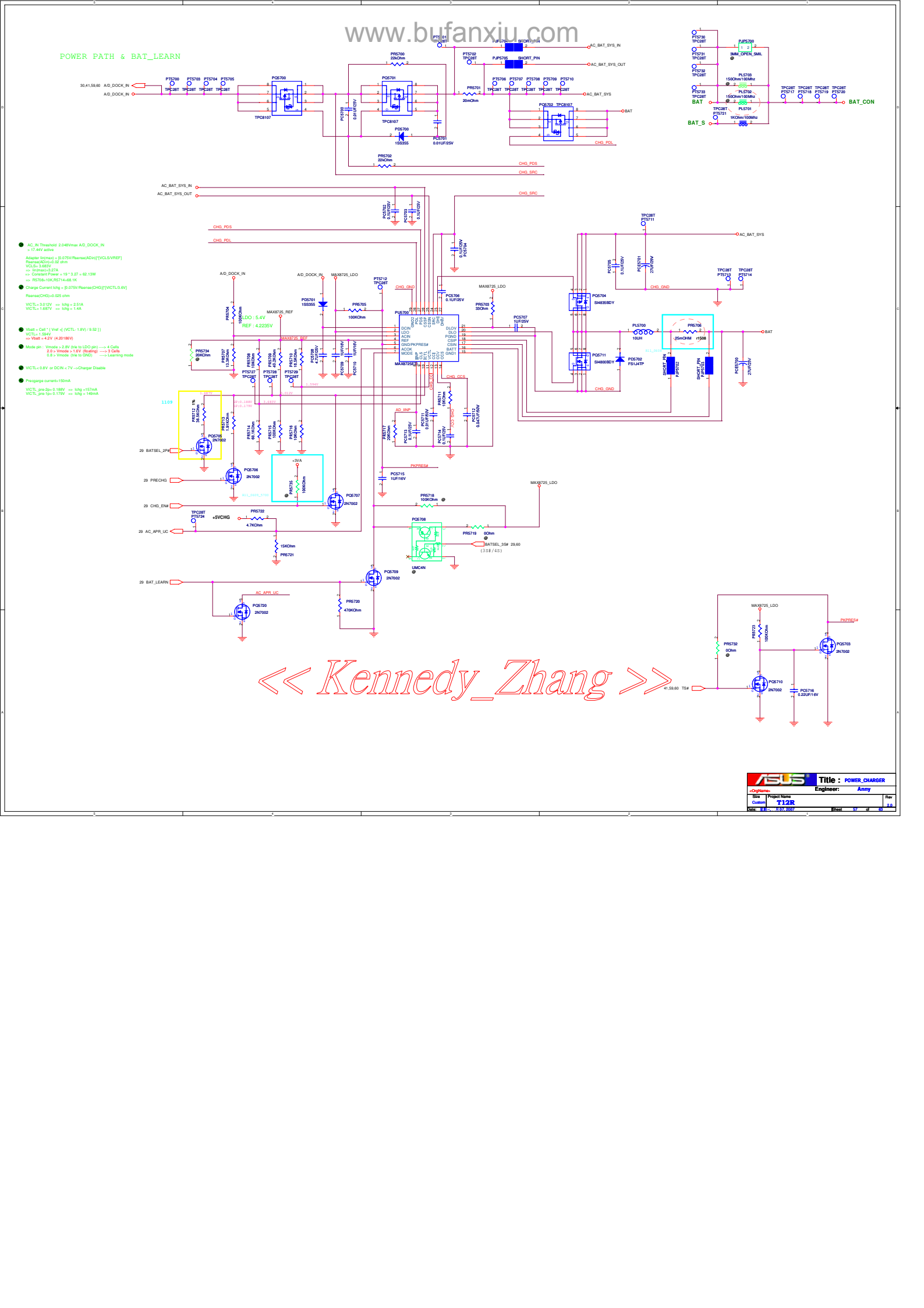
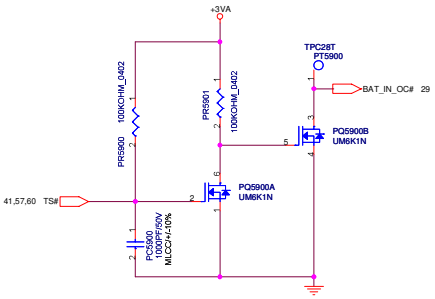
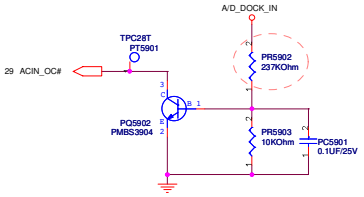


Title : POWER_CHARGER			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
Date: 三月 07, 2007	Sheet 57 of 68		

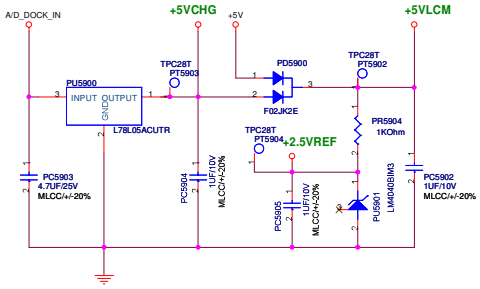
BATTERY IN DETECT



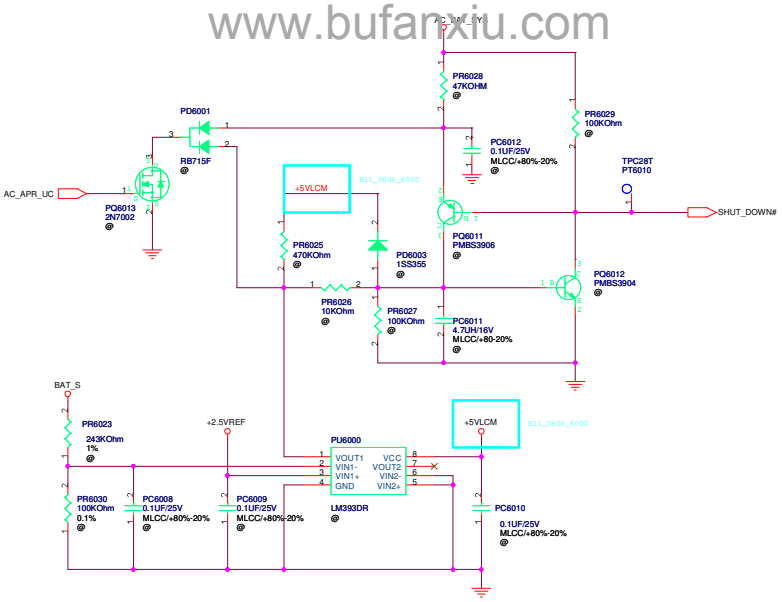
ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF

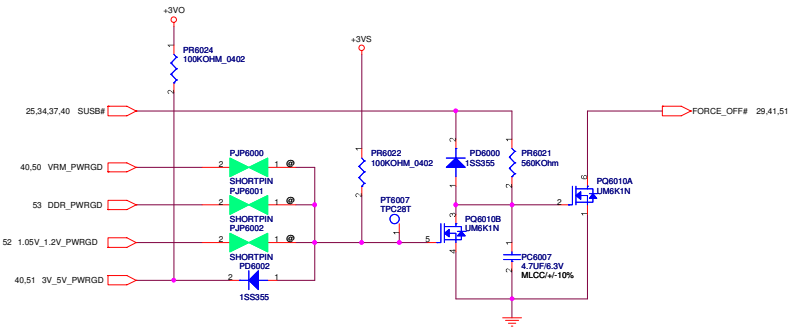


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: 星期一, 四 07, 2007	Sheet 59 of 63	



	8.575V	11.625V
R6023	243KOhm 10G2132433130 30 1%	365KOhm 10G2133653130 10 1%
R6024	100KOhm 10G2131003230 10 0.1%	100KOhm 10G2131003230 10 0.1%

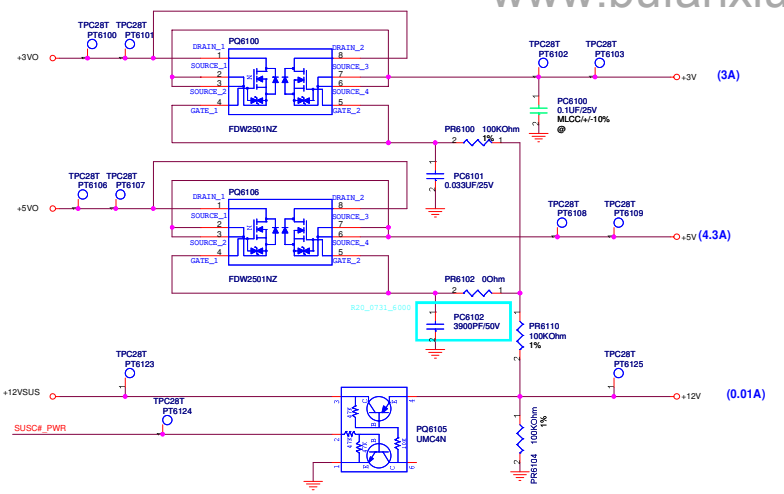
POWER GOOD DETECTER

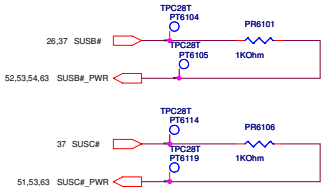


TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.2V_PWRGD

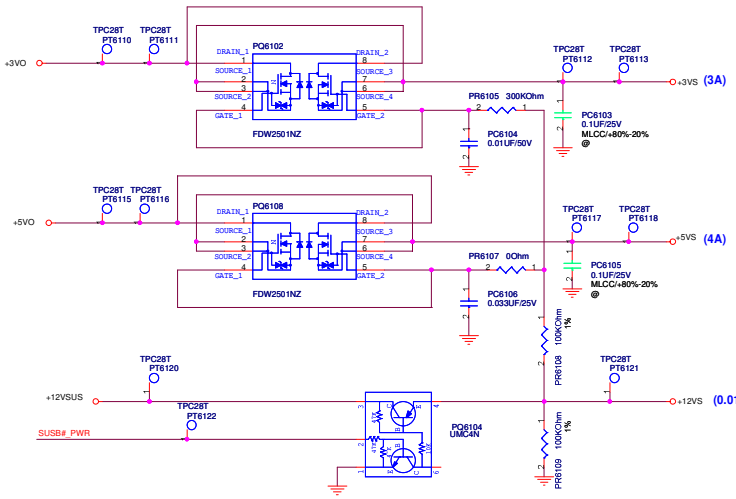
ASUS	Title : POWER_PROTECT		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 60 of 63		

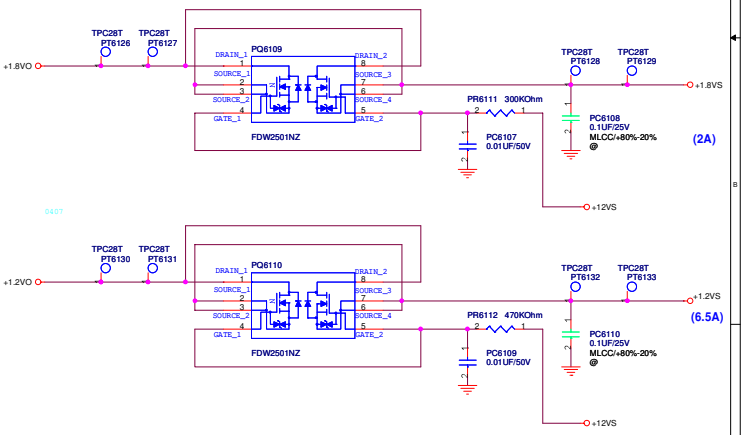
SUSC#_PWR POWER





SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 61 of 63		

AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA → +3VA 4,12,20,22,29,37,38,40,54,59

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 18,19,20,25,29,34,40,51

+5VSUS → +5VSUS 20,30,51,60

+3V → +3V 12,18,26,27,31,37,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 36,37,54,61

+12VS → +12VS 12,22,27,33,37,61

+5V → +5V 9,12,30,36,37,44,59,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,37,38,50,61

+1.2VO → +1.2VO 52

+1.2VSUS → +1.2VSUS 52

+1.2VS → +1.2VS 61

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,37,53

+VCCP → +VCCP 2,6,9,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH → +VCCP_GMCH 9,10

+VCCP_ICH → +VCCP_ICH 17,20

+0.9VS → +0.9VS 16,37,53

BAT → BAT 30,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 57,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST

+3VA → PJP6300 (SGL_JUMP, @) → CPU_VRON_PWR 50

PJP6301 (SGL_JUMP, @) SUSB#_PWR → SUSB#_PWR 52,53,54,61

PJP6302 (SGL_JUMP, @) SUSC#_PWR → SUSC#_PWR 51,53,61

PJP6303 (SGL_JUMP, @) VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 63 of 63	

R2.0

Item	Before	After	Reason	Owner	Date
R20_1109_50		Add PCE5001 PCE5005, PQ5002, PQ5004, PQ5005 and PQ5007	VCORE:CPU upgrade to merom reflash		2006.11.09
R20_1109_50	9.31K	11K	VCORE: PR5030 modify to 11K to Increase OCP.		2006.11.09
R20_1109_57	PR5712 and PQ5705 were unmounted	PR5712:36.5K and PQ5705 was mounted.	Charger: Modify PR5712 and PQ5705 for 3S1P select.		2006.11.09

ASUS Title : POWER_PIC

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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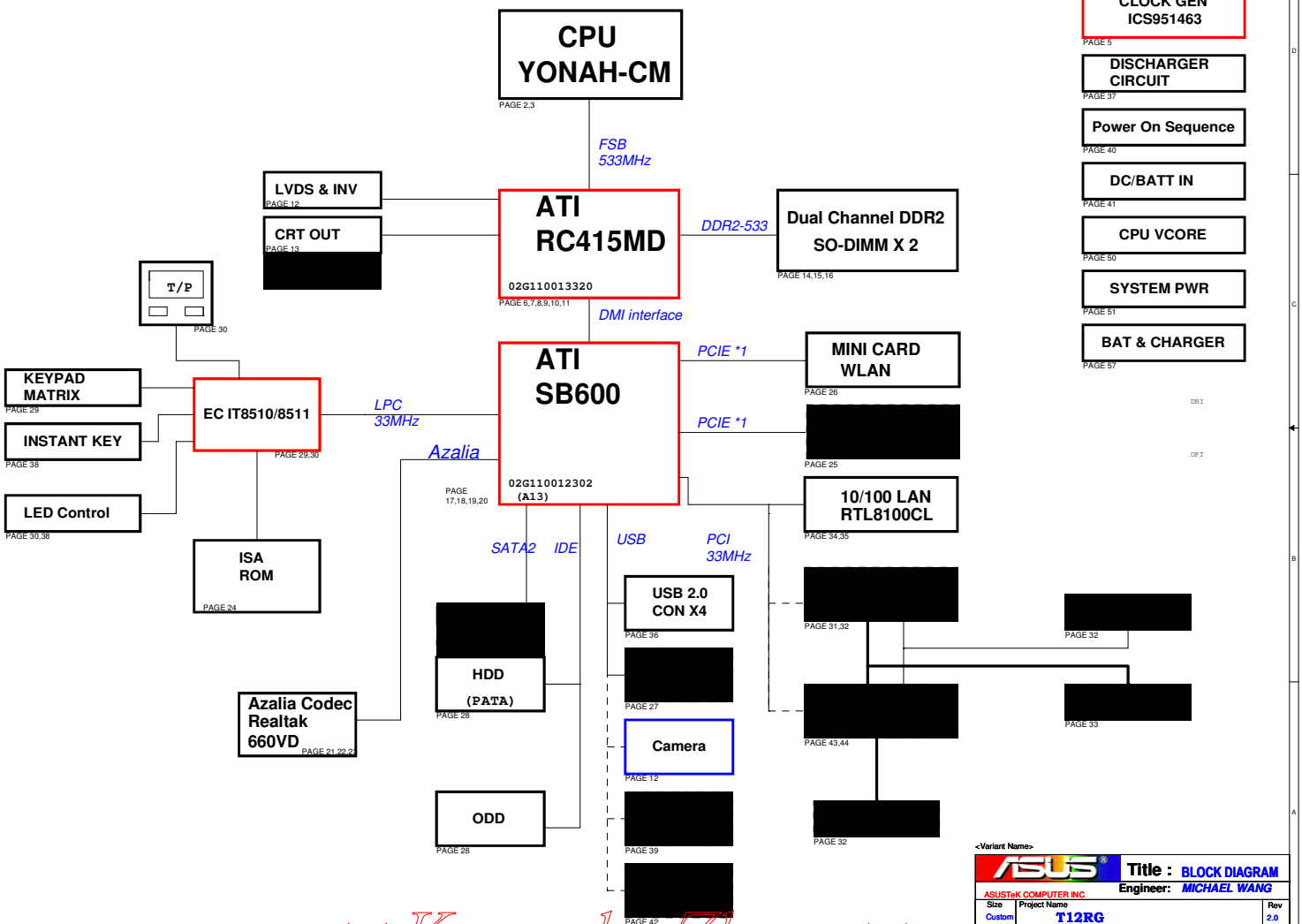
T12Rv Block Diagram V2.0



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

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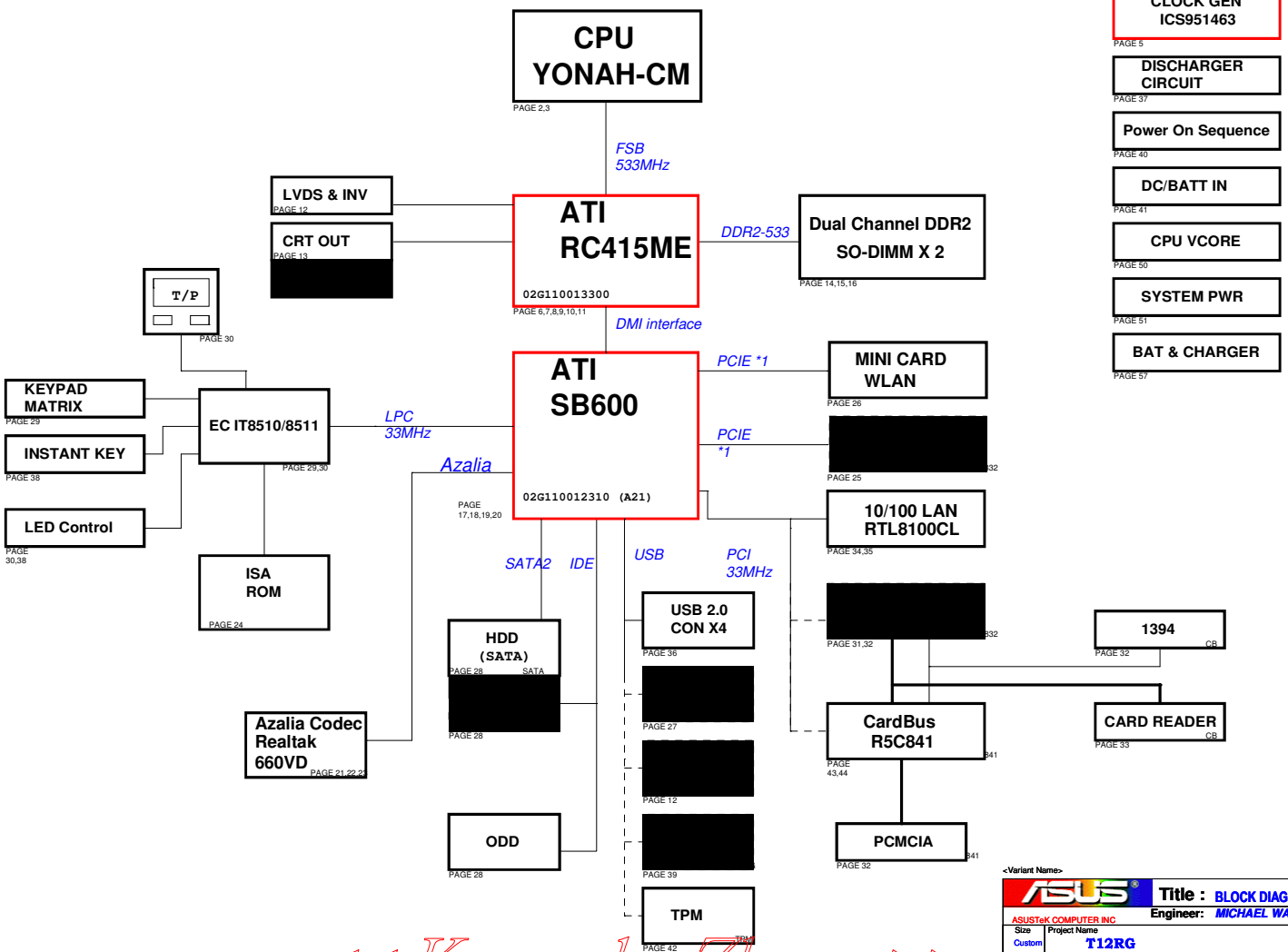
T12Rg Block Diagram V2.0



<Variant Name>

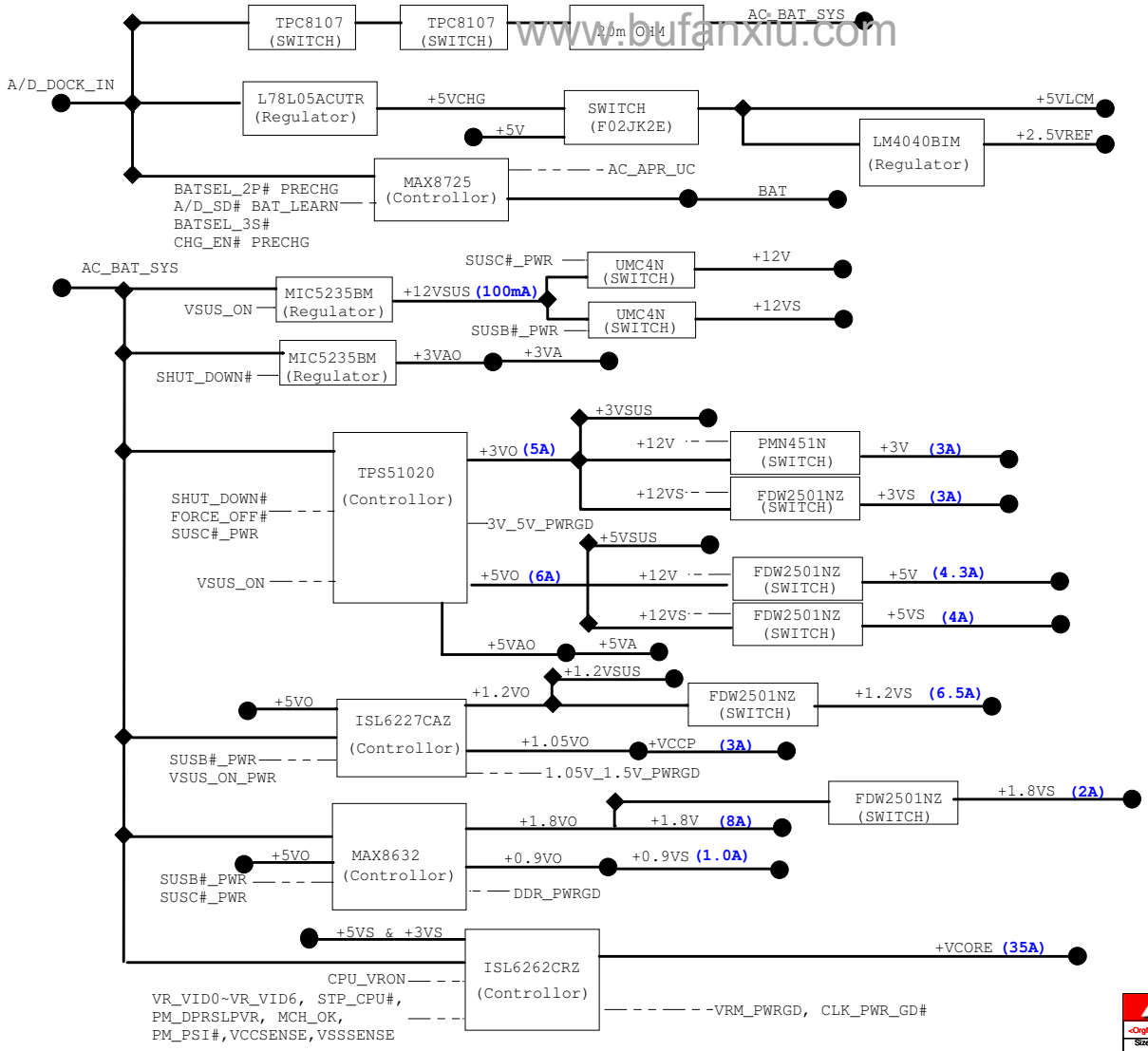
Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期三, 二月 07, 2007 Sheet 72 of 63



Title : POWER_FLOWCHART
Engineer: Anny
<OrgName>
Size: Custom
Project Name: T12R
Rev: 2.0
Date: 星期二, 一月 07, 2007
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